Analog Signal Processing Products

Where Vision and Technology Meet

Reticon Corporation's leadership in the application of semiconductor technology to analog signal processing and optical image sensing problems is undisputed. We started strong in 1971 and maintain our position today for four important reasons.

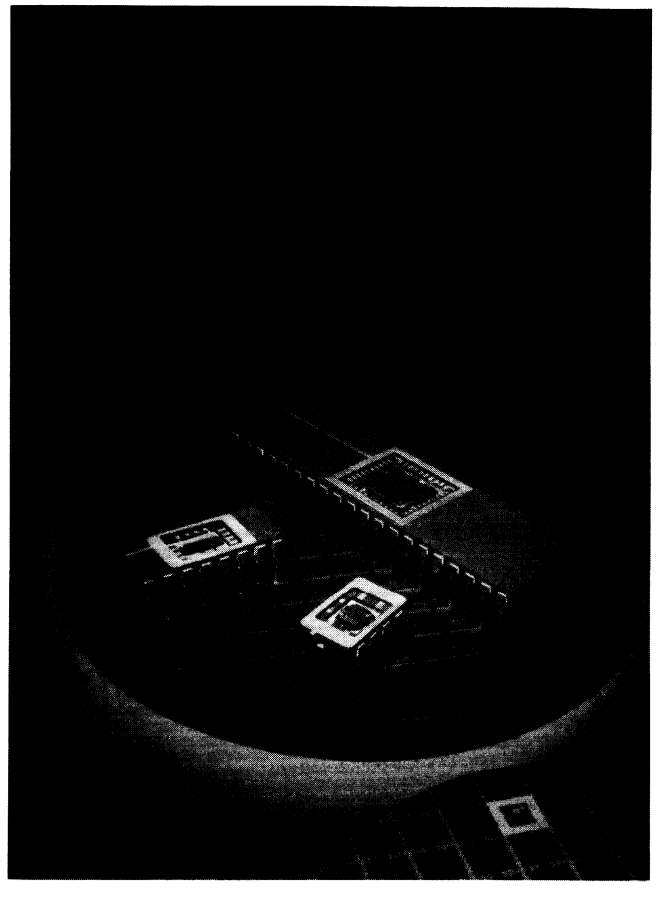
Our people - the pioneers
Our senior engineers were among the first to produce practical photodiode array and integrated analog circuit designs. Since then our designers' personal drive to advance the state-of-the-art and commitment to creative solutions to our customers' application problems have produced an impressive list of technological firsts.

Our philosophy - keep moving forward
We became the industry leader because we had the first practical designs and the first commercial products. We continue to dominate our markets because, while others are content to modify existing technology, we move forward. Our mission is to create new technology that produces powerful products which solve problems in unprecedented ways while reducing size, weight and cost.

Our resources — the finest
Evidence of our commitment to excellence is visible throughout our physical plant. Sophisticated computer-aided design facilities, a state-of-the-art wafer fabrication plant, and a comprehensive product testing lab are incisive reminders of manufacturing follow-through for innovative designs.

Our product line — diverse and extensive
Reticon's list of available photodiode arrays and monolithic analog signal processing devices is larger than that of all other manufacturers, combined. A solution to your design problem probably already exists; if it doesn't, we are ready to explore custom design possibilities with you.

We also manufacture Reticon Solid State Camera products, applying photodiode array technology to industrial process monitoring and control problems. Precise non-contact measurement, automatic process control and hostile environment monitoring are among the uses of our cameras, their associated controllers and computer interfaces.



The potential for application of Reticon Analog Products is limited only by the imagination of our OEM customers.

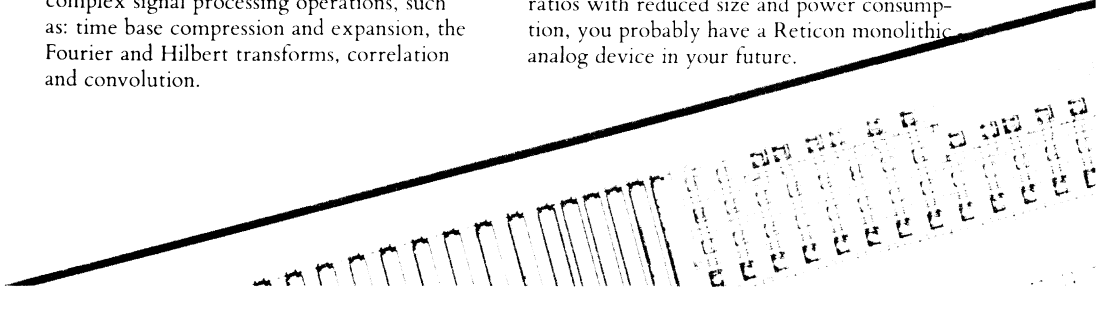
Monolithic Analog Devices

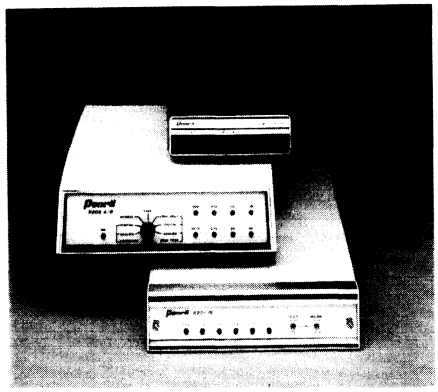
Reticon applies N-channel Metal Oxide Silicon technology to complex analog signal processing problems. We design and produce charge transfer devices and switched capacitor filters that perform all of the classic signal processing functions in small, inexpensive packages.

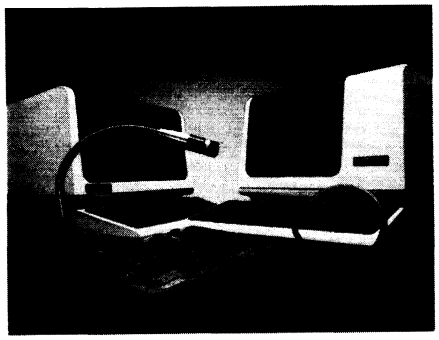
We have a solution for you, no matter what your filtering problem: lowpass, highpass, bandpass, notch or programmable. Other Reticon integrated circuit devices perform complex signal processing operations, such as: time base compression and expansion, the Fourier and Hilbert transforms, correlation and convolution.

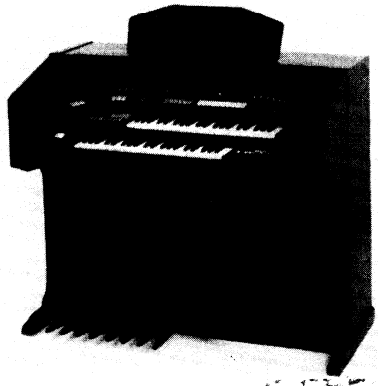
Our engineers wrote the book on switched capacitor filter design and implementation. Reticon's design pioneers established their leadership early and, since then, our list of contributions to the state-of-the-art remains unequalled.

A Reticon integrated circuit will perform at least as well as its discrete or hybrid equivalent while conserving circuit board real estate, weight, power and money. So, if your goals include improved cost/performance ratios with reduced size and power consumption, you probably have a Reticon monolithic analog device in your future.









Left:
Custom switched-capacitor filters assure accurate data transmission through the Penril 300/1200 modem.
Below:
Another filter pack enables Interstate's speech recognition system to add new dimensions to data entry, security and other computer-aided activities.
Bottom:
General Electro Music uses Reticon's analog delay to create various musical effects, such as chorusing and vibrato in their electronic organs.

Reticon Analog Firsts

Year	Description
1977	Commercial analog-analog correlator chip
1977	Commercial binary-analog correlator chip
1977	Fully integrated, tapped delay transversal filter (TAD32)
1978	Commercial Chirp-Z Fourier signal processing chip (R5601)
1978	Commercial general purpose switched capacitor filter
1979	Commercial switched capacitor modem filters
1979	Fully integrated, programmable universal active filter (R5620)
1981	Fully integrated, commercial voice recognition filter set
1981	300 Baud modem filter, Bell 103 and V.21 compatible (R5630/1)
1982	1200 Baud modem filter, 212/V.22 compatible (R5632)

Analog Signal Processing Products

Reticon offers a broad line of integrated circuits which are used to perform discrete-time or sampled-data signal processing. Figure 1 shows the general family of Reticon products and capabilities.

All of these devices perform the discrete-time processing by storing sequential samples of the input signal as packets of charge. Figure 2 shows the functional diagram of a typical sampled data system. Such a system quantizes the time but not the amplitude of the samples. These stored charge samples are then shifted through the device by multiphase clocks to produce the basic signal processing operations of delay, multiplication, and addition. By combining these operations appropriately, complex signal processing functions such as time compression and expansion, filtering, correlation, convolution, and the Fourier transform can be achieved. With the same technology, classical active filters are synthesized utilizing the "switched capacitor (SCF) architecture."

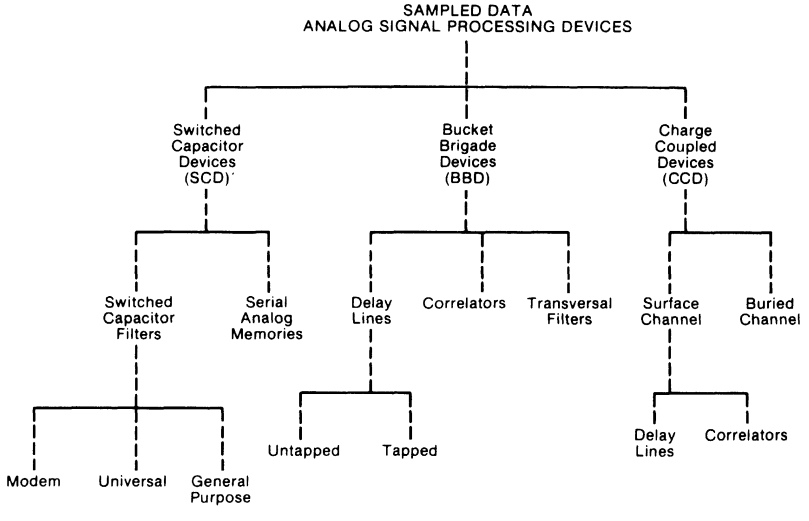


Figure 1.

DEVICE TECHNOLOGY

SWITCHED CAPACITOR FILTERS (SCF)

Switched capacitor filters can implement the classical discrete functions of allpass, bandpass, notch, highpass, and lowpass filtering and the familiar responses of Chebyshev, Butterworth, Bessel, Cauer, etc. Resistors and inductors are replaced by sampled data integrators composed of a switched capacitor and an integration capacitor connected across an all-MOS op-amp. Figure 3 shows the switched capacitor network building block: an integrator which replaces an RC product with a capacitance ratio (C_2/C_1) and a toggle switch frequency (fs).

The advantages of SCF devices are reduced circuit complexity, low sensitivity to coefficient variations, clock tunability of center/corner frequencies, and reduced silicon area. The stability of SCF's eliminates alignment problems, thus removing the need for tight-tolerance components and trimpots or laser trimming. Since multiple filters (up to 100 poles) can be designed for a single-chip package-a savings in circuit board real estate-manufacturing insertion, testing and inventory costs will also be realized.

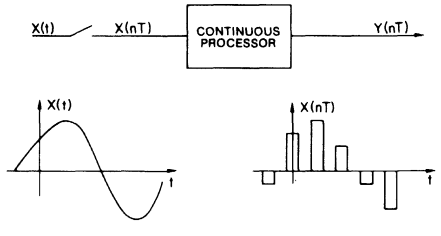


Figure 2. Sampled Data System

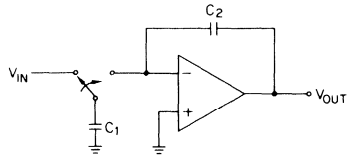


Figure 3. The switched-capacitor integrator looks like an analog resistor only if fs, the toggle frequency, is rapid enough

CUSTOM and MASK-PROGRAMMABLE SCF's

Low-cost customized filter responses are available by modification of a single mask layer used in device fabrication. For example, a 7-pole elliptical lowpass filter can be modified to become a 7-pole Butterworth, Chebychev, or an elliptic with a new response.

Fully customized devices are also available for applications in modems, voice processing, sonar and many others. Most classical designs can be duplicated within the following constraints:

Parameter	Limit
Output Voltage	12 volt p-p, max
Filter Center/Corner	100KHz, max*
Sample Rate	3MHz
Input Impedance	>100K ohms
Output Impedance	<1K ohm
Number of Poles	Up to 100 per chip
Q	<100

* Upper limit dependent on values of Q.

CHARGE TRANSFER DEVICES (CTD)

CTD devices are implemented using two similar but structurally different integrated circuit technologies. Figure 4 shows the "Bucket Brigade" device or BBD. These devices are basically a series of MOS transistors and storage capacitors. The charge is transferred from one capacitor to the next by the alternate switching of the MOS transistors. All Reticon BBD's are fabricated using n-channel silicon gate technology with a tetrode-gate configuration and selective ion implantation.

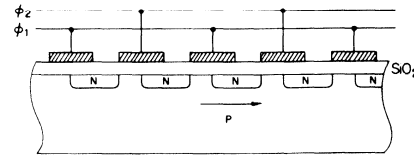


Figure 4. Bucket Brigade Device

A second category of CTD's is the Charge Coupled Device (CCD). The basic principle of CCD operation centers around the storing of mobile minority charge carriers in the depletion region under a pulsed electrode. The electrodes are spaced closely together (See Figure 5) such that when they are pulsed by the clocks, an array of overlapping potential wells is formed allowing the charge to move in the direction of the deepest or lowest-energy potential well. Reticon CCD's use an n-channel four phase clocking electrode structure.

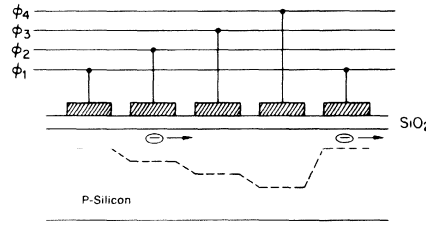


Figure 5. 4 Phase Charge Coupled Device

PRODUCT DESCRIPTIONS

SWITCHED CAPACITOR FILTERS

R5630 300 BAUD MODEM FILTER

The R5630 is a full duplex, originate/answer SCF modem compatible with 103/113 type modems. The device contains two 10-pole switched-capacitor bandpass filters fabricated using well-established NMOS technology and packaged in a single 16 pin DIP (See response diagram in Figure 6).

Switching the filters between originate and answer modes is accomplished by a mode-select pin which is TTL-compatible. Included on the chip are a receive gain control stage (externally adjustable from 0 to 20dB), a separate limiter for use with the receive output, a TTL compatible input for self-test mode, and an on-chip oscillator. The R5630 was designed to operate with an external 1MHz crystal or clock, in conjunction with various commercially available mod/demod devices.

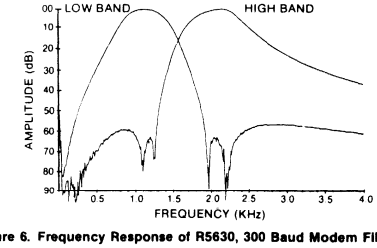


Figure 6. Frequency Response of R5630, 300 Baud Modem Filter

R5631 V.21 MODEM FILTER

The R5631 is designed for the 200/300-baud CCITT V.21 application and is exactly pin-for-pin compatible with the R5630 modem filter chip. Its characteristics are identical

to those of the R5630 except for the specific filter parameters needed for V.21. This is a valuable and cost-effective companion to the R5630 for those who supply modems, both to the U.S. and CCITT countries.

R5632 212/V.22 MODEM FILTER

The R5632 is a Full-Duplex, 1200 Baud Modem Filter Chip, containing two SCF sets fabricated using NMOS double-poly technology. Each filter set contains a ten-pole bandpass filter and a ten pole allpass section which provides the accepted compromise line equalization to improve data quality in 212-compatible modems.

For CCITT V.22 application, selectable guard-tone notch filters at 550Hz and 1800Hz are included with greater than 45dB of rejection.

The bandwidths and group-delay variations of the low- and high-band filters are 960Hz and ± 100 μsec respectively.

R5620, R5621, and R5622 UNIVERSAL PROGRAMMABLE ACTIVE FILTERS

These filters may be configured to form any classical filter type—lowpass, bandpass, highpass, notch, or allpass. The R5620 is programmable electrically by a digital selection code, without external components. The R5621 and R5622 are programmable by selection of external resistors. All are tunable by clock rate control as well as by programming.

The R5620 is particularly effective where filter characteristics must be changed rapidly or electrically. The R5621 has two second order sections, the R5622 has four.

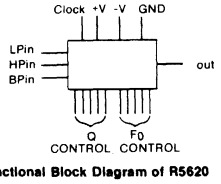


Figure 7. Functional Block Diagram of R5620

R5604, R5605, R5606 ANSI OCTAVE BANDPASS FILTERS

This family consists of 1/3-octave ANSI Class III (R5604) (see Figure 8), 1/2-octave ANSI Class III (R5605) and full octave ANSI Class II (R5606) filters which are used extensively in audio spectrum analysis. These filters meet ANSI types R, E and O specifications for center frequencies up to 10 KHz. By utilizing switched-capacitor architecture for these sampled-data filters, the center frequency scales with the sampling frequency.

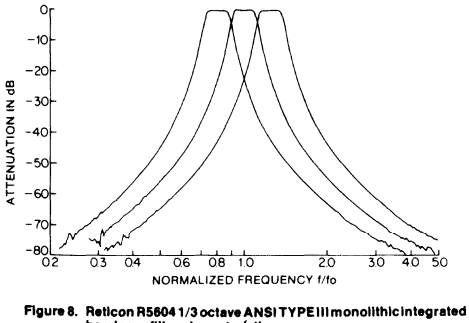


Figure 8. Reticon R5604 1/3 octave ANSI TYPE III monolithic integrated bandpass filter characteristics

R5614, R5615, and R5616 HIGH FREQUENCY ANSI OCTAVE BANDPASS FILTERS

The filters are monolithic 6-pole ANSI Class III third-octave, half-octave and, full-octave filters clock tunable to greater than 20 KHz. Each is housed in an 8-pin mini-DIP package. Dynamic range is better than 86 dB and signal handling capability is greater than 17V p-p.

R5609, R5611, R5612, and R5613 FILTERS

Tunable elliptical lowpass (R5609), notch (R5612), highpass (R5611), and linear phase lowpass (R5613) filters are available for a variety of applications at signal frequencies approaching 25 KHz. These SCF devices feature packaging in an 8-pin mini-DIP with identical pin-outs. The center/corner frequency is clock adjustable. (See Figure 9 for the lowpass filter responses.)

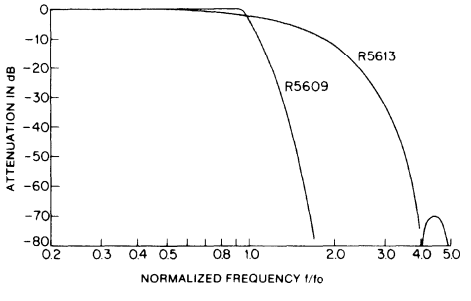


Figure 9. Magnitude response of R5609 and R5613 switched-capacitor filter

BUCKET BRIGADE DEVICES (BBD)

AUDIO DELAY LINES

By performing a time delay on an analog signal, many useful applications can be realized which can save money, effort, and board space.

Various musical effects such as tremolo, vibrato, chorusing or flanging can be achieved by feedback and clock modulation. Other music applications include echo, reverberation, and ambience (sound enhancement).

Other analog delay-line applications are in data compression, voice actuated switches, speech scrambling, beam forming, data buffering, pitch correction, and many others.

SAD1024A SERIAL ANALOG DELAY

The SAD1024A is a dual 512 [illegible]256 sample) audio delay line (see Figure 1[illegible] [illegible]lent performance characteristics, wi[illegible] [illegible] dynamic range when measure[illegible] [illegible]d less than 1% distortion. Eac[illegible] [illegible]t and has two stages per samp[illegible] [illegible]e through each half is equal to 256 div[illegible] [illegible]e sample frequency with a minimum of 256 [illegible] and a maximum of about a 100

DISCONTINUED
Replaced by
R5107.

milliseconds at room temperature. The signal bandwidth is equal to 35% of the sample frequency, but has a maximum of 200 KHz. Operation can also be by serial connection, parallel-multiplex or by differential operation of two sections. Various musical effects such as vibrato or flanging can be achieved by feedback and clock modulation. The SAD1024A is also used in such applications as data compression and as a voice actuated switch.

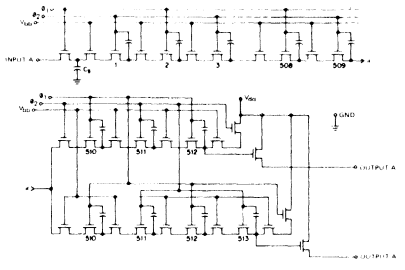


Figure 10. Equivalent Circuit Diagram of Either 512-Stage Section of the SAD-1024A

SAD512 SERIAL ANALOG DELAY

The SAD512 is identical to SAD1024A. It contains only one section. It is useful where only a single delay section. It slightest crosstalk or even the package would be a common

DISCONTINUED
Replaced by
R5106.

R5106 SERIAL ANALOG DELAY WITH DRIVER

The R5106 is similar to the SAD512 except that it contains an on-chip clock driver and thus requires only a single-phase, 5-volt clock input. It is intended for high-volume low-cost applications where performance is important. It is capable of sample rates up to 1 MHz, a dynamic range of 70 dB and a throughput gain of approximately unity. It has similar applications to the SAD1024A and SAD512.

SAD4096 SERIAL ANALOG DELAY

For very long delay the SAD4096 offers a 2048 sample delay. It is functionally equivalent to 4 SAD1024 devices in series. The SAD4096 is ideal where a large delay-bandwidth product is required.

DISCONTINUED
Replaced by
two R5108's.

TRANSVERSAL FILTERS

R5602A Transversal Filter

The R5602A mask-programmed filters are a family of 64 stage BBD devices available with various filter functions. A standard family of lowpass (R5602A-1), bandpass (R5602A-3), and chirped filters (R5602A-7, 8) is available. These filters can be made with linear phase response and with skirts greater than a 150 dB/octave roll off rate. Sampling rates of 1 MHz and an ultimate rejection in the stopband of typically 50 dB makes it ideal for use in high speed modems, matched filters, correlators and tracking filters. Translation of the filter characteristic is done by a change of the clock frequency. The response of the R5602A-1 lowpass filter is shown in Figure 11.

In addition, custom devices can be designed to meet individual requirements. Calculated tap weights for custom devices can be verified using the TAD-32A. This is analogous to verifying digital codes in PROM before committing them to a mask programmable ROM.

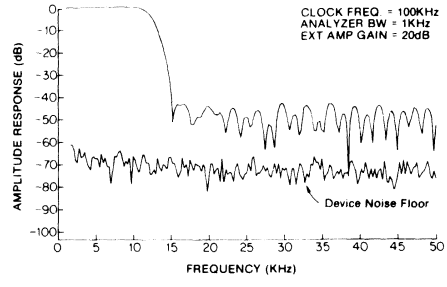


Figure 11. R5602-1 Narrow Lowpass Filter Spectral Response

R5602A-7, R5602A-8 SINE/COSINE CHIRPED TRANSVERSAL FILTER

The R5602A-7, 8 is a single 64 point chirped transversal filter that is similar in performance to the R5601A except four individual devices are required. This device is available with Hanning windows.

TAPPED DELAY LINES

TAD32A TAPPED ANALOG DELAY

The TAD32A is a thirty-two stage delay line with an output at each stage. The outputs come from two source followers, one from each element of the stage (see Figure 12) to give a full-wave output with reduced clock modulation.

Each tapped output is delayed one sample time from the preceding one. In addition, there is a feed-forward output to allow multiple devices to be cascaded. Many signal-processing applications are possible with the most obvious being transversal filters, recursive filters and correlators. When used as a transversal filter (no feedback), external resistors are connected to the outputs to form the tap weight function. The TAD32A is capable of sampling rates from 1 KHz to 5 MHz and dynamic ranges greater than 60 dB.

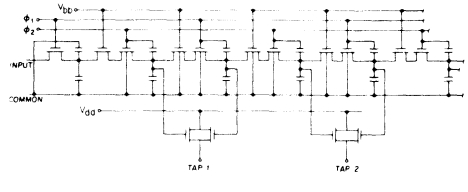


Figure 12. A tapped analog delay line made using metal-oxide-silicon integrated circuit technology

SUMMARY OF SIGNAL PROCESSING DEVICES

	Clock Rate (MHz)	Typical Signal to Noise (dB)	Pkg Pins	Evaluation Circuit	Description
DELAY LINES					
R5106	1.5	70	8	SC5106	256 sample BBD delay line w/driver & S/H
R5107	1.5	70	8	SC5106	512 sample BBD delay line w/driver & S/H
R5108	1.5	65	8	SC5106	1024 sample BBD delay line w/driver & S/H
SAD512	1.5	70	16	SC1024A	Single 256 sample BBD delay line (use R5106 for new designs)
SAD1024A	1.5	70	16	SC1024A	Dual 256 sample BBD delay line, replaced by R5107
SAD4096	2	70	16	SC4096	2048 sample BBD, replaced by two R5108
SWITCHED CAPACITOR FILTERS					
R5604	2	80	16	N/A	3 ⅓ octave Class III band-pass
R5605	2	80	16	N/A	2 ½ octave Class III band-pass
R5606	2	80	16	N/A	1 full octave Class II band-pass
R5609	2	80	8	N/A	7th order elliptic low-pass
R5613	2	80	8	N/A	Linear Phase Low-pass
R5611	2	80	8	N/A	5th order Chebyshev high-pass
R5612	2	80	8	N/A	Notch
R5614/15/16	1	90	8	N/A	20KHz ⅓, ½, full octave band-pass
MODEM FILTERS[2]					
R5630	1	75	16	N/A	103/113 Compatible modem, full duplex
R5631	1	75	16	N/A	V.21 Compatible modem, full duplex
R5632	0.1536	70	24	N/A	212/V.22 Compatible modem, full duplex
R5633	1.5	70		N/A	General Purpose, 103/V.21/Bandsplit/Videotex
UNIVERSAL ACTIVE FILTERS[2]					
R5620	1 ^	84-94	18	N/A	Digitally Programmable Universal Active
R5621/22	.75	98	14/20	N/A	Resistor Programmable Universal, Two and Four 2nd order, respectively
R5626	1	85	24 +	N/A	Semi-custom Mask Programmmable SCF array, up to 28 poles
TRANSVERAL FILTERS (DFT/Matched Filter Applications)					
R5601A-1	2	40-60	22	RC5601	Quad chirp filter (CCD), 512 stages, unwindowed
R5601A-2	2	40-60	22	RC5601	With Hanning Window
R5602A-1	1	40-60	16	N/A	Low-pass, 64 taps
R5602A-3	1	40-60	16	N/A	Band-pass, 64 taps
R5602A-7	1	40-60	16	N/A	Sine Chirp with Hanning Window
R5602A-8	1	40-60	16	N/A	Cosine Chirp with Hanning Window
TAD32A	5	60	40	TC32A[1]	32 equally spaced output taps (BBD)

NOTES: (1) Three versions available. Specify desired type by dash number, -01 has fixed tap weight resistors, -02 adjustable taps using potentiometers and -03 without resistors.
(2) Switched capacitor filter.

CHARGE COUPLED DEVICES (CCD)- Surface Channel

CHIRPED TRANSVERSAL FILTERS (DFT/Matched Filter Applications)

R5601A QUAD CHIRPED TRANSVERSAL FILTER

The R5601A performs the convolution portion of the chirp Z algorithm to perform either a Discrete Fourier Transform (DFT) or the power spectral density of the input signal in real time. A block diagram of these functions is shown in Figure 13.

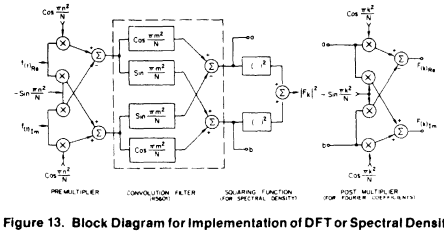


Figure 13. Block Diagram for Implementation of DFT or Spectral Density

The R5601A is available with a rectangular (R5601A-1) or Hanning (R5601A-2) window function. The R5601A-1 can be used to implement either the total DFT or the power spectral density while the R5601A-2 can only do the power spectral density. Each R5601A contains four 512-tap split electrode transversal filters, two sine and two cosine chirps. The device takes in 512 time samples and outputs 512 coefficients. It is capable of sampling the input signal at rates up to 2 MHz.

Reticon also has a circuit board which performs the entire function. The RC5601 board can operate to 100 KHz and has an output accuracy of 7 bits. Applications are numerous as the Fourier transform is a basic tool for signal processing. Some application areas are in voice analysis, bandwidth compression, vibration analysis, instrumentation, radar, and communications.

Reticon has produced a variety of experimental and custom production signal processing devices, such as binary-analog correlators, analog-analog correlators, MUX's, beam formers, transversal filters, adaptive equalizers, signal averagers, and many others. Reticon is continually looking for new, innovative ways to solve its customers' application problems, either with custom or standard products.

Applications include modems, voice processing, sonar processing, DFT spectrum analysis, spread spectrum processing, and noise analysis.

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Analog Signal Processing Products

EG&G RETICON R5106 SAMPLED ANALOG DELAY LINE (Pin-compatible replacement for SAD512D)

Key Features

- 512-element delay
- On-chip driver requiring only single TTL-level clock input
- Clock-controlled delay: more than 1 sec to less than 300 μsec
- Improved N-channel silicon-gate bucket-brigade technology
- Sample-and-hold output circuit for maximum self-cancellation of clocking modulation
- Wide signal-frequency range: 0 to more than 300 KHz
- Wide sampling clock frequency range: 0.25 KHz to more than 500 KHz
- Wide dynamic range: S/N >70 dB
- Low distortion: less than 1%
- Single 12 volt power supply (5 to 13 volts range)
- 8 pin mini DIP

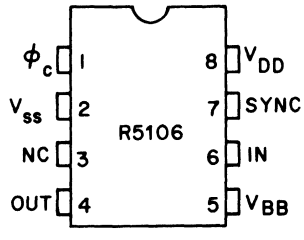


Figure 1. Pinout, R5106

R5106 Sampled Analog Delay Line

The R5106 is a general-purpose Sampled Analog Delay device fabricated using N-channel silicon gate technology in a bucket-brigade configuration. It is an improved pin-compatible replacement for the SAD-512D.

Typical Applications

- Voice control of tape recorders
- Control of equalization filters
- Reverberation effects in stereo equipment
- Tremolo, vibrato, or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Time compression of telephone conversations or other analog signals
- Voice scrambling systems
- Storage of multi-level digital signals

Device Description

The R5106 is a 512-element Bucket Brigade Device (BBD) with internal clock drivers that require only a TTL-level (or higher) single-phase clock input (f_C).

A sampled-and-held output is provided for smooth stair-step output over each full clock period in normal operation. The R5106 is manufactured using an improved N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket-brigade charge-transfer device. It is packaged in a standard 8-lead dual-in-line package with pin configuration as shown in Figure 1. The functional equivalent circuit is shown in Figure 2.

Drive and Voltage Requirements

Normal voltage levels and limits are given in the tabular specifications. The clock input is a rectangular wave which controls the on-chip drivers. The magnitude of the clock may be any positive pulse voltage from 2 volts to V_{DD}. The phase relationships of clock input, sync input (when used) and output waveforms are shown in Figure 4. The input trigger clock is best as a controlled rectanguiar puise with rise and fall times less than 50 nsec. For operation at the highest frequency, it should be a square wave, but more generally, the positive portion should have a duration greater than 200 nsec (preferably greater than 500 nsec) and the low-level portion should be greater than 300 nsec. Within these broad limits, the timing is non-critical. The positive portion determines the duration of the sampling period of the output sample-and-hold so that short pulses give a cleaner output step. The low-level portion determines the input tracking interval, of minor importance so long as the duration is great enough (preferably 300-500 nsec or greater).

For optimum performance, V_{DD} is 13 volts and V_{BB} approximately 10 to 10.5 volts. However, for battery or portable operation, both may be operated at lower levels. V_{BB} is internally derived from V_{DD}, but requires an external load of approximately 20KΩ to V_{SS} (ground) to give the desired relationship between V_{DD} and V_{BB}. The input bias voltage is best derived as a (large) fraction of the V_{BB} voltage, as in the circuit sketch, Figure 3; when so derived, operating conditions track with minimum or no readjustment when V_{DD} changed, even over a wide range.

When used, the sync input should be a postive pulse of magnitude $V_{DD}/2 < V_{sync} \leq V_{DD}$, and timing as shown in Figure 4; that is, the sync input should rise 50 nsec or later after a falling edge of the trigger clock input, and fall at or before the next falling edge of the trigger clock.

If the sync input is unused, pin 7 should be connected to ground.

As with all sampled-data devices, the input bandwidth should be limited to a value less than one-half the sampling clock frequency (usually to a value less than 0.3 f_S). Further, to recover a smooth delayed analog output, a post filter having steep cutoff (e.g., 36 dB per octave or more) is desirable.

Performance

Typical performance of the device is shown in the specifications and in the curves of Figures 5 through 7. These data were obtained with the test configuration on Figure 4 or similar. Sampling waveforms, propagation delays, and internal dispersion become the limiting factors for sampling clock frequencies above 800 KHz (1.6 MHz f_C).

Figures 5 and 6 indicate the linearity and show the rapid increase in distortion as the input level is increased toward saturation. For inputs less than approximately 1.5 volts rms, the distortion is less than one percent. Between this point and the noise floor, there is approximately 75 dB of dynamic range. This dynamic range assumes an A weighting filter and a sample rate of 100 KHz or faster. With a 20 KHz filter and 50 KHz sample rate, the dynamic range is 70 dB. Broad-band dynamic range is better than 60 dB for all sample rates.

The output is internally sampled and held, then buffered by a source follower with internal load adequate to drive a capacitive load of up to 200 pF without further components. With 200 pF, the slew rate is approximately 0.5V/μsec, and is inversely proportional to the capacitance load. The slew rate is limited by the internal pull-down current of approximately 150 μA; pull up is at least an order of magnitude faster (lower in impedance). The internal current is inadequate to drive a low a-c coupled resistance without substantial increase in second harmonic. A-C coupled loads are preferably 50K or greater. Otherwise, an external buffer as in the circuit of Figure 9 is recommended.

The sampled-and-held nature of the output signal implies a frequency response of the form $[\sin(\pi f_m/f_s)]/(\pi f_m/f_s)$ independent of any transfer gain or loss of the delay line itself (f_m is the signal frequency and f_s the sample frequency). This response function is simply the amount of equivalent base-band signal in the stair-step sampled signal. Figure 7 shows its relative attenuation

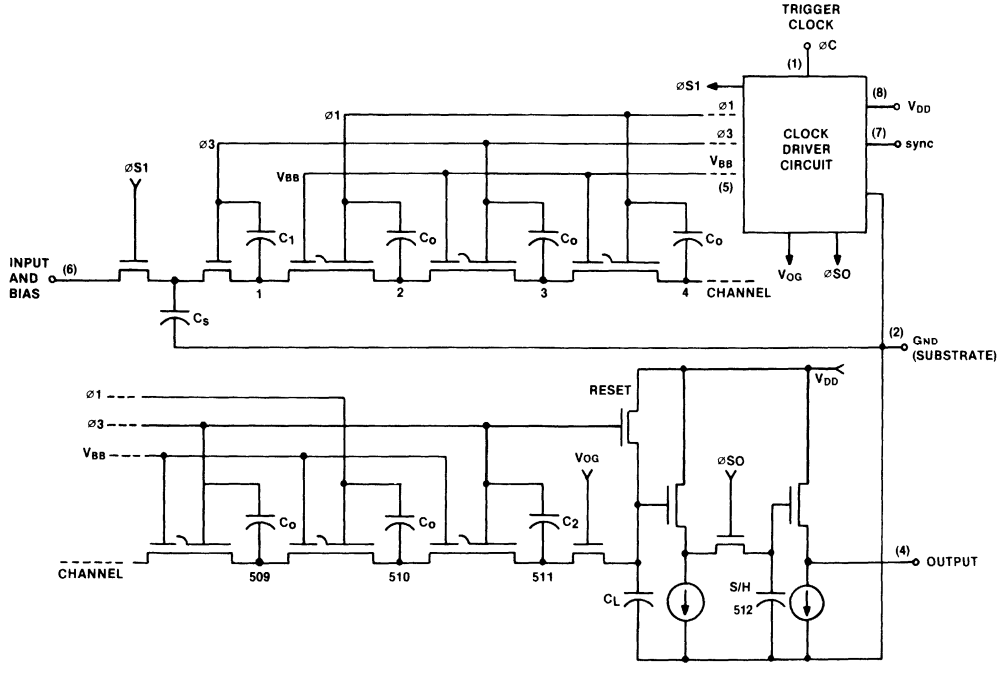


Figure 2. Equivalent Circuit of R5106

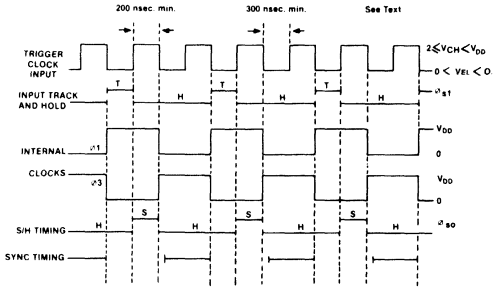


Figure 3. R5106 Timing Relations

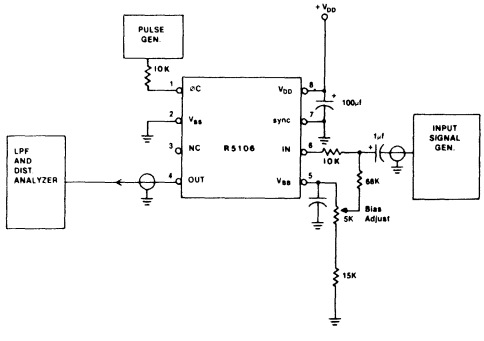


Figure 4. R5106 Test Configuration

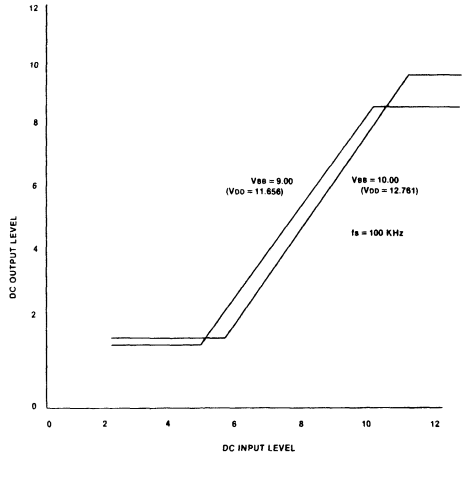


Figure 5. DC Output vs. DC Input, R5106

as a function of f_m/f_s. It also shows typical performance of the R5106 for various sample rates ($f_s = f_c/2$), including the effects of f_m/f_s. Note that, typically, there is less than 1 dB loss in the delay line itself.

Circuit Configuration

The normal operating configuration is shown in Figure 9. The bias should be set such that sine-wave signals large enough to show visible clipping are symmetrically clipped; the clipping should disappear on both top and bottom as the signal level is reduced. A different device, or operation at different sample rates (particularly for changes between widely different sample rates) may require readjustment for optimum performance.

A sync input is included on the device and the waveform is shown in Figure 4. This input allows synchronized operation of multiple devices in either serial or parallel configuration when the same sync pulse is applied to each individual R5106. If the devices are used individually, the sync input (pin 7) should be grounded.

Performance Considerations

The R5106, because of its low cost and clock-fixed delay independent of input frequency, has many applications in the consumer area, particularly for providing delay and its associated effects for audio-frequency devices (e.g., reverberation, vibrato, speed change or corrections, etc.). It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on control of the clock frequency.

The analog input should be filtered to limit input components to less than $f_{sample}/2$. Normally a stricter limiting is desirable-to a limit more nearly 0.3 f_{sample}. The reason for this requirement is that all input components become modulated by the sampling frequency to generate (f_s-f_m) and also many other products. The result is to "fold" the input about $f_s/2$ so that components above $f_s/2$ reappear on equal distance below $f_s/2$. Limiting the input to $f_s/3$ provides a filter "guard band" to permit adequate attenuation of the otherwise disturbing high-frequency components.

The output should be filtered because, even after the S/H, the output is only stepwise continuous. Clocking steps appear at the times of clock transitions. The high frequencies contained in the abrupt changes are all extraneous and for best performance should be removed by a filter with cut-off at approximately $f_{sample}/2$ or less and rolloff of as much as 36 dB/octave or more. One can move the cutoff frequency by scaling the resistor or capacitor values, or their products (e.g. to double the cutoff frequency to 30 KHz, one halves the resistance or capacitance value). If simple RC filtering is used, note that the output impedance of the R5106 is quite high.

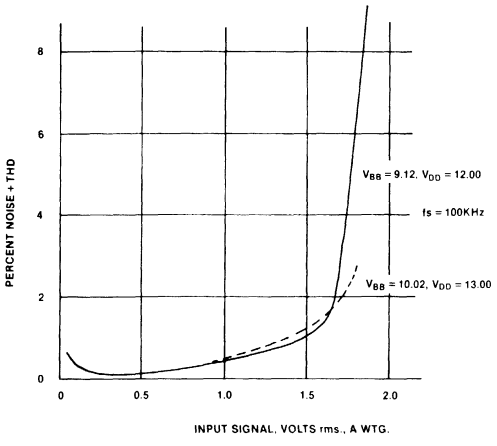


Figure 6. Total Harmonic Distortion + Noise vs. Input Level

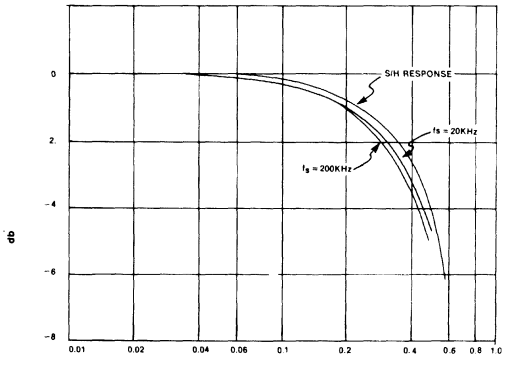


Figure 7. Relative Responses of R5106 vs. Sample Rate, fs

Therefore, the loading impedance should never be less than 100KΩ; otherwise, second order harmonic distortion will become excessive. A simple PNP emitter follower with an Re of 12KΩ will insure a high loading impedance. Also, overload should be avoided because increased signal amplitude near overload gives rise to rapidly increasing high-order intermodulation products which lie within the useful pass band and which thus are not normally reducible by output filtering.

For optimized performance, care should be given to layout and design as well as the filtering requirements. Ground planes are generally required on circuit boards to reduce cross-talk, and shielding of high-impedance circuits, such as the input circuit, is desirable.

For many applications, cost is a more important factor than the ultimate in performance, and relaxed filtering is permissible. However, the user should be well aware of the cost/performance tradeoffs involved.

Evaluation Circuit SC5106

For evaluation purposes or for relatively high-performance operation, a circuit board is available from Reticon. This board encompasses the required filters, operation amplifiers, and ground plane. The schematic is shown in Figure 9. The board provides a variable oscillator for sample frequencies from 20 KHz to 200 KHz. The output filter amplifier is designed as a two-pole, maximally flat filter with a cutoff frequency of 15 KHz. Change in cutoff frequency requires component changes.

The SC5106 board is designed to handle a wide range of bandwidths and clock rates; as a consequence anti-aliasing input filters should be externally provided to limit the input bandwidth to less than $f_{sample}/2$.

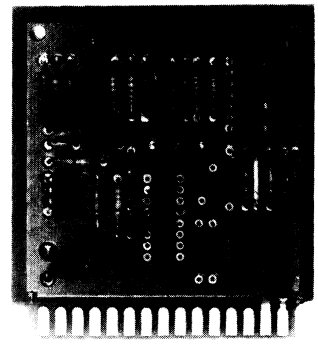


Figure 8. SC5106 Evaluation Circuit

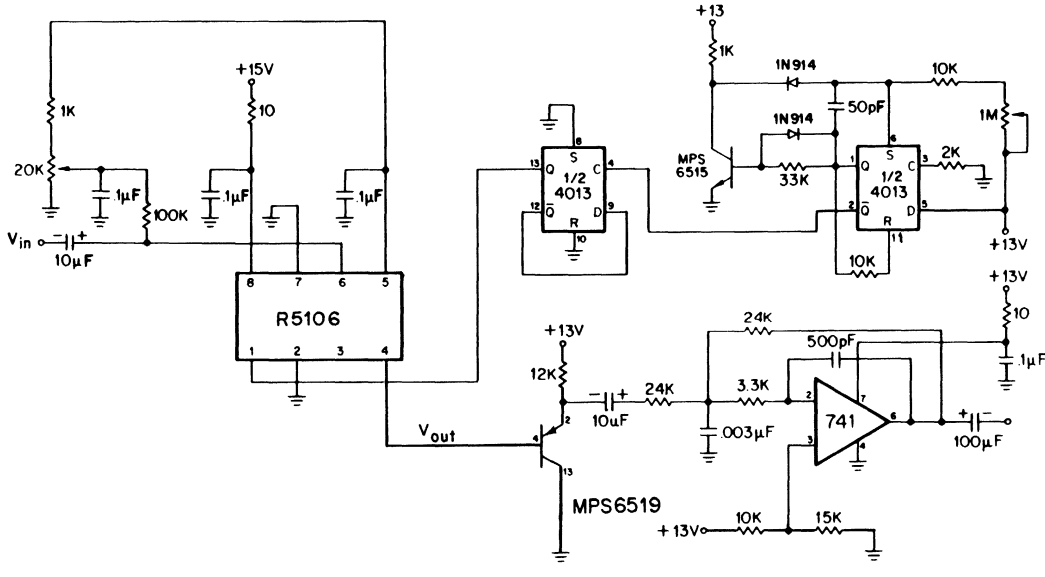


Figure 9. SC5106 Evaluation Circuit Schematic

Table I

Absolute Maximum Rating	Min	Max	Units
Voltage on any terminal with respect to common	-0.4	+18	V
Storage Temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

Caution

Static discharge to any lead of this device may cause permanent damage. Store with shorting clip or inserted in conductive foam. Use grounded soldering irons, tools, and personnel when handling devices. Avoid synthetic fabric smocks and gloves. It is recommended that the device be inserted into socket before applying power. Power supplies should not exhibit turn-on or turn-off spikes. Use decoupling networks to suppress power supply turn on/off transients, ripple and switching transients. Do not apply independently powered or AC coupled signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken.

Table II
Device Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Trigger Clock Voltage Amplitude[1]	V_C	2		V_{DD}	Volts
Drain Supply Voltage[1]	V_{DD}	5	12	13	Volts
Tetrode Gate Voltage (see text)	V_{BB}		V_{DD}-2	V_{DD}	Volts
Sampling Frequency (½ External Clock Frequency)	f_S	0.25	50-100	800	KHz
Clock Pulse Width	t_{cp}	200	$t_C/2$	t_C-300	nS
Signal Frequency Bandwidth (3 dB point)		See Fig. 8	$0.4f_S$		
Signal to Noise		See Fig. 5			
Distortion		See Fig. 6			
Gain[2]		0	3		dB
Input Capacitance	C_{in}			15	pF
Input Shunt Resistance[3]	R_{in}	300			Kohms
Optimum Signal Input Bias[4]			7.6		Volts dc
Maximum Input Signal Amplitude[5]		1.0	1.5		Volts rms
Sync Pulse Amplitude		5		V_{DD}	Volts
Clock Input Capacitance	Cc		8	10	pF

Notes: 1. All voltages measured with respect to GND (pin 2).
2. The value of gain depends on the output loading. Values given are for limited external loading.
3. Effective a-c shunt resistance measured at ½ MHz sample rate.
4. The input bias voltage varies with the magnitude of the clock voltage (and V_{DD}) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 12 volt clocks.
5. With V_{DD} = 13V, V_{BB} 10.4, f_S = 100 KHz.

Advance Data
R5107 AND R5108
ANALOG DELAY LINES

General Description

The R5107 and R5108 are general purpose sampled analog delay devices configured with a bucket brigade charge transfer mechanism. They are fabricated in a double poly NMOS silicon gate technology and are packaged in a single 8 pin mini-DIP.

Along with the R5106, the R5107 and R5108 form a new family of pin compatible delay lines.

The user can conveniently increase his delay time by merely interchanging devices in the same socket and printed circuit board.

The R5107 is a 1024 element delay (512 samples) and the R5108 is a 2048 element delay (1024 samples). The delay is controlled by the clock frequency, f_C, according to the relationship $T_D = 1024/f_C$ (R5107) and $T_D = 2048/f_C$ (R5108).

The R5107 is an improved and smaller (8 pin mini-DIP versus 16 pin DIP) replacement for the SAD1024A. Although they are functional equivalents, the package and feature differences prohibit interchangeability. Two of the R5108's (8 pin mini-DIP) are the functional equivalent to the SAD4096 (16 pin DIP), with the advantage of a center tap. For detailed operating specifications, refer to the R5106 data sheet.

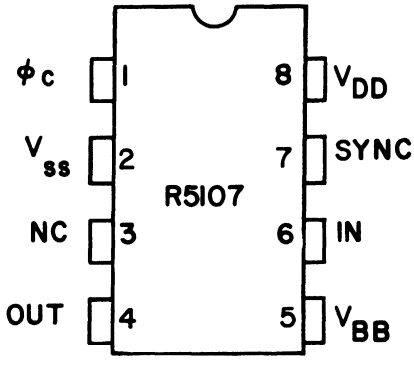


Figure 1. Pinout

Key Features

- On-chip clock driver with input requiring only a low-level voltage swing (TTL, CMOS).
- Sample-and-hold output for maximum self-cancellation of clocking modulation.
- Sampling clock frequency range ($f_S = ½ f_C$): 1KHz to more than 800KHz.
- Dynamic range: S/N >70dB.
- High signal-frequency range: 0 = D.C. to more than 300KHz.
- Single 12 volt power supply (5 to 13 volt range).

Applications

- Convenient A.G.C. control
- Voice control of tape recorders
- Tremolo, vibrato, or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Time compression of telephone conversations or other analog signals
- Storage of multi-level digital signals
- Voice scrambling systems

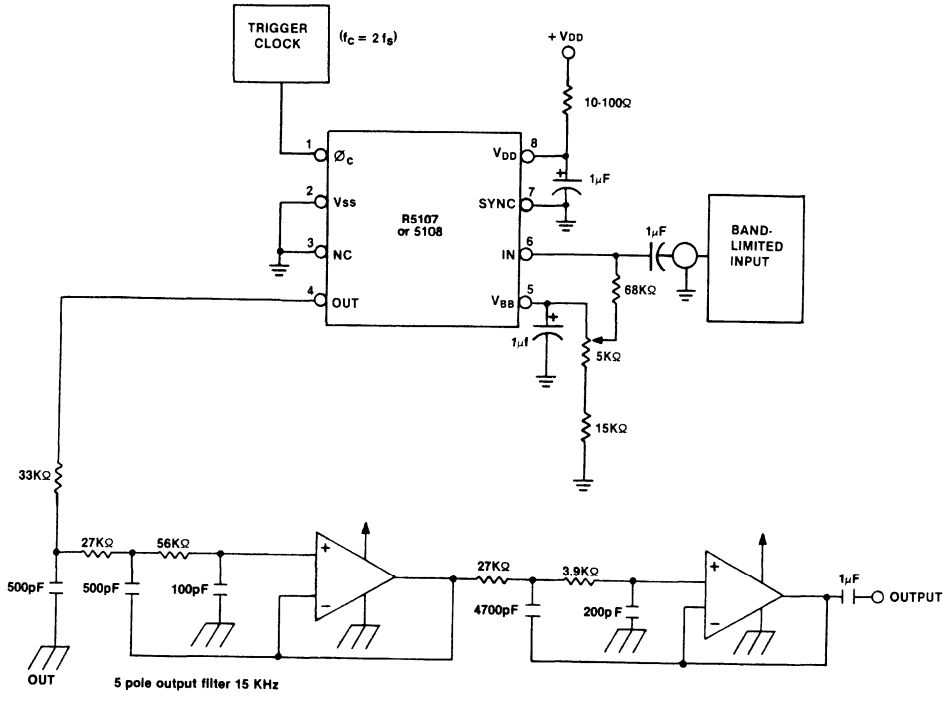


Figure 2. Typical Circuit

Analog Signal Processing Products

R5604/R5605/R5606
1/3, 1/2, FULL OCTAVE BAND-PASS FILTERS

Description

The Reticon R5604, R5605, and R5606 are monolithic switched-capacitor band-pass filters in 16 pin DIP's.

The R5604 contains three (6-pole Chebyshev) 1/3 octave ANSI Class III filters that together cover an entire octave using one external input clock trigger.

The R5605 contains two (6-pole Chebyshev) 1/2 octave ANSI Class III filters that together cover an entire octave using one external input clock trigger.

The R5606 contains one (6-pole Chebyshev) full octave ANSI Class II filter.

The center frequency of all filters is tunable by the clock frequency. The dynamic range is better than 80 dB and distortion is less than 0.1%. The filters will handle input signals of greater than 10 volts p-p. The filters have an insertion loss of less than ±0.2 dB.

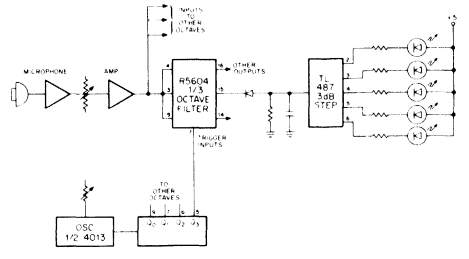


Figure 1. 1/3 octave spectrum analyzer.

Typical Applications

- Spectrum analysis (parallel or swept filters)
- Audio filtering
- Noise analysis
- Equalization
- Harmonic analysis

An equivalent inductor-capacitor (LC) circuit is transformed into a leap-frog configuration for use in the integrated circuit. The building blocks used in the leap-frog schematic are realized using switched-capacitor integrators.

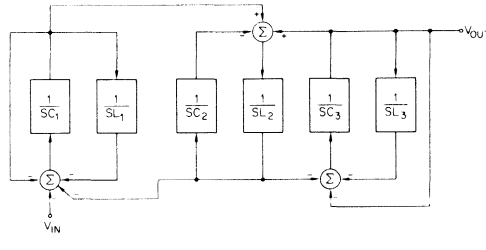


Figure 4. Filter realization-active leap-frog technique.

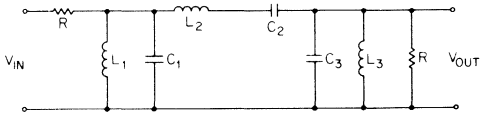


Figure 2. L-C circuit equivalent to the switched capacitor filters.

Device Operation

The R5604, R5605, and R5606 are self-contained and require only an external clock trigger and plus and minus power supplies to operate. The device characteristics and operating parameters were obtained for the R5604 using the test configuration shown. The same configuration with appropriate pin number changes was used for the R5605 and R5606.

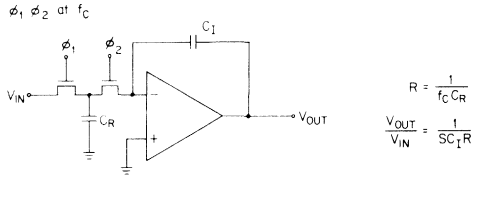


Figure 3. Switched capacitor resistor integrator used in the leap-frog filter realization.

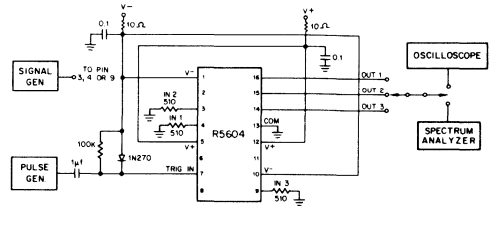


Figure 5. Test circuit for the switched capacitor filters; pin connections shown are for the R5604.

Antialiasing Considerations

The sampling rate on the R5604, R5604, and R5606 filters is approximately 54 times the filter center frequency. As in all sampled data systems, signals above half the sampling frequency (fs) will be aliased and may appear in the band of interest. If signals greater than 27 fo will be applied to the filter, an external antialiasing filter may be required. A typical 2-pole antialiasing filter with design equations is shown below. In applications where the clock residue may affect system performance, a single pole filter should be added to the filter output. Typical clock residue is 25 mV p-p.

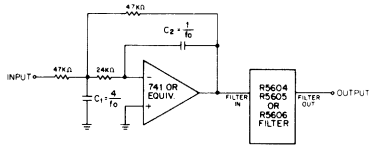


Figure 6. Antialiasing filter for use with R5604/R5605/R5606 filters.

Note that the input trigger clock frequency, f_C, is twice the sample rate, or approximately 108 times the center frequency. The input clock rate is divided by two in generating the on-chip clock waveforms which control the sample rate, fs.

Custom Devices

Most classical polynomial and ladder filter designs can be duplicated within the following restraints:

Parameter	Limit
Maximum Output Voltage	12 Volt p-p
Maximum Filter Center Frequency	50 KHz
Maximum Sample Rate	3MHz
Input Impedance	⩾100KΩ
Output Impedance	⩽1KΩ
Number of Poles	Up to 100 per chip
Q	⩾100

Switched capacitor filters have several design advantages over conventional techniques. The most obvious is the ability to integrate several filters of one or more types into a single IC. The filters can also be built to tolerances on the order of 1.0% or better.

Since multiple filters can usually be designed on a single chip a savings in circuit board real estate, manufacturing insertion costs, testing costs and inventory costs will be realized.

The stability of the switched-capacitor filters eliminates alignment problems thus eliminating the need for tight tolerance components and trimpots.

Table I
Absolute Maximum/Minimum Ratings*

	Min	Max	Units
Input Voltage-any terminal with respect to substrate[1]	-.4	21	V
Output short circuit duration-any terminal	—Indefinite—		
Input/Output current-any terminal externally forced[2]		10	mA
Power Dissipation[3]	500		mW
Storage Temperature-plastic	-55	125	°C
Operating Temperature-plastic	0	70	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

***Caution:** Observe MOS Handling & Operating Procedures*
**Operation at these limits may result in permanent damage.*

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{QDD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

Table II
Device Characteristics

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Input Impedance	Ri	3			Megohms
Input Capacitance	Ci			20	pF
Dynamic Output Impedance	Ro			10	ohms
Maximum Output Capacitive Load		50			pF
Trigger Clock Input Capacitance	C_C			10	pF
Positive Supply	V+	5		10	volts
Negative Supply	V-	-5		-10	volts
Clock Trigger Voltage[1] [2]	Vc	2.2		V+	volts
Trigger Pulse Width	Tcp	200		tc-200	nS
Center Frequency	fc	0.5		20,000	Hz

Table III
Performance Specifications*

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Clock to Center Frequency Ratio	fc/fo (=2 x fs/fo)	52	54.5	57	
Q: R5604 R5605 R5606		4.50	4.70 3.00 1.48	4.80	
Supply Current	I_D		8		mA
Maximum Output Current	Io	2			mA
Output Voltage Swing	Vo		17		volts p-p
Output Noise[2]			0.35	0.4	mV_{rms}
Dynamic Range[3]			86	95	dB
Total Harmonic 17Vp-p Distortion[3] @ 2 KHz 2Vp-p				0.5 0.1	%
Power Supply Rejection V+ (to 50 KHz) Subt V- (20 KHz/50 KHz			 40 30/25		 dB
Insertion Loss		-0.2	0	0.2	dB
Pass-band Ripple			.20	.50	dB

1. All devices are internally gate protected for static immunity. Applying AC signals or clock to chip with power off may exceed negative limit.
2. Trigger voltage is CMOS/TTL.
3. Broad band to 1/2 the sample rate.
4. V = ± 10V, fo = 2KHz

*V+ = 10V V− = −10 v F_O = 2 KHz 25°C

Table IV
ANSI Specifications for Typical 3 dB Bandwidth and Minimum 40 dB Rolloff

		3 dB Bandwidths		40 dB Bandwidths	
	FO	LOW	HIGH	LOW	HIGH
Third Octave Filter	1	0.89	1.11	0.64	1.52
Half Octave Filter	1	0.62	1.19	0.51	1.96
Full Octave Filter	1	0.72	1.40	0.31	3.29

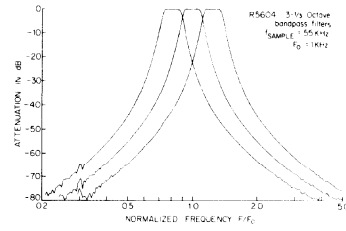


Figure 7. Frequency response, R5604.

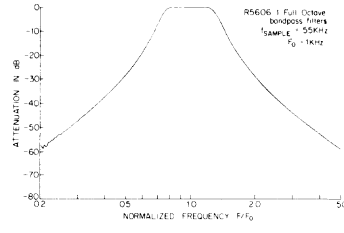


Figure 8. Frequency response, R5605.

Table V
Pin Connections for R5604, R5605 and R5606

PIN	R5604 FUNCTION	R5605 FUNCTION	R5606 FUNCTION
1	V-	V-	V-
2	N/C	N/C	N/C
3	IN 2	IN 1	N/C
4	IN 1	N/C	N/C
5	V+	V+	V+
6	N/C	N/C	N/C
7	TRIG IN	TRIG IN	TRIG IN
8	N/C	N/C	IN 1
9	IN 3	IN 2	V-
10	V-	V-	N/C
11	N/C	N/C	N/C
12	V+	V+	V+
13	COM	COM	COM
14	OUT 3	OUT 2	N/C
15	OUT 2	N/C	N/C
16	OUT 1	OUT 1	OUT 1

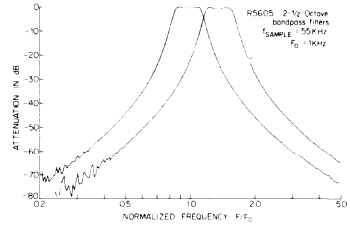


Figure 9 Frequency response, R5606.

Key Features

- Easy to use
- No external components required
- Small size: 8 pin mini-DIP
- Wide power supply range: ±5V (or 10V) to ±10 (or 20V)
- Dynamic Range: up to 75 dB
- Corner Frequency Range: 10 Hz to 25 KHz
- Insertion loss: 0 dB

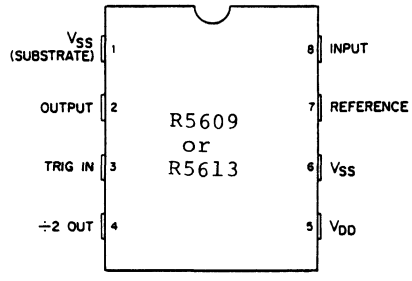


Figure 1. Pinout

Description

The Reticon R5609 and R5613 are monolithic switched-capacitor low-pass filters fabricated in a double-poly NMOS process.

The R5609 is a seven-pole, six-zero elliptic low-pass filter with over 75 dB out-of-band rejection and less than ±0.5 dB of passband ripple. The Reticon R5613 is a linear-phase low-pass filter with over 60 dB out-of-band rejection. It has an elliptic stop band response for faster rolloff.

The stability of the switched-capacitor filters eliminates alignment problems and the need for tight tolerance components and trimpots.

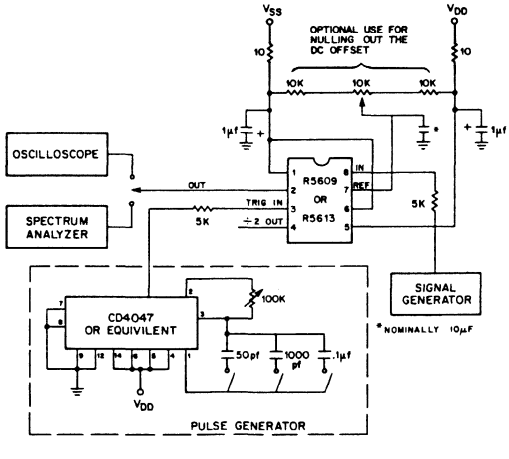


Figure 2. Test circuit

Note: The following should be applied in test and production circuits as applicable. (See Table I)

1) Power supply resistors may be required for transient protection.

2) Input and trigger resistors are required if signals or trigger may be applied with power off, and there is not a resistor already in series with the input or trigger.

Typical Applications

- Antialias filters
- Reconstruction filters
- Tracking filters
- Audio analysis
- Telecommunications
- Portable instrumentation
- Biomedical/Geophysical instrumentation
- Speech processing

Device Operation

The R5609 and R5613 are self-contained and require only an external clock trigger, either TTL or CMOS, and power supply. The device characteristic and operating parameters were obtained using the test configuration shown in Figure 2.

In applications where DC information must be passed through the filter, the output offset may be nulled out by varying the reference voltage, which will change the input trigger level and may require adjustment of clock voltage values. The reference input requires less than 100 µA of current and must always be well-filtered. A circuit that may be used to adjust out the output offset is shown as optional resistors in Figure 2.

A divide-by-two output is also available. This output contains a square wave at the sample rate and may be used for triggering, summing out the sample rate residue, or driving additional filters especially when filtering requirements are spaced by an octave. Gain and phase tracking from device to device and over the temperature range is typically better than .5%. This measurement excludes the fixed offset of fc/fo tolerance at room temperature.

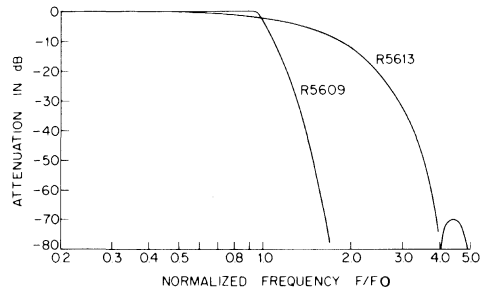


Figure 3. Magnitude response

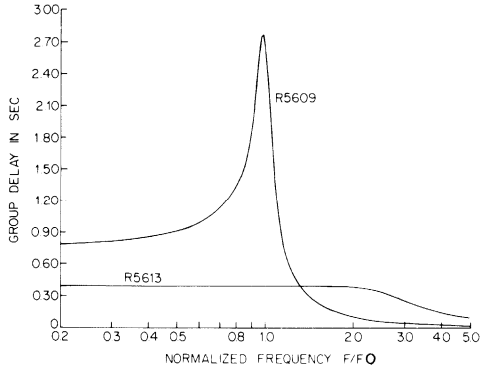


Figure 4. Group delay

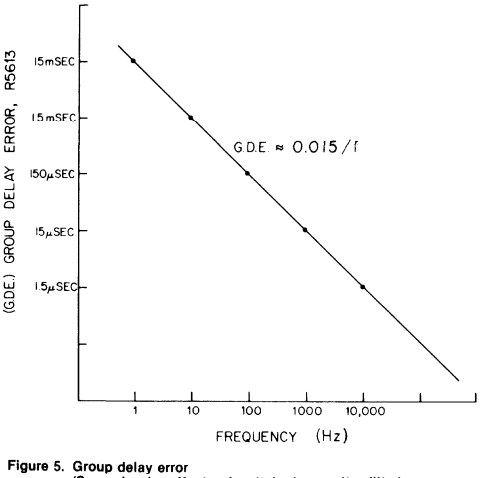


Figure 5. Group delay error
(Second order effects of switched capacitor filter)

Pre/Post Filtering Considerations

The typical sampling rate on the R5609 is 50 times the corner frequency and for the R5613 it is 64. (Note: Sampling rate = ½ input clock trigger rate.) Because these sample rates will be far from the frequencies of interest in most cases, antialiasing filtering will usually not be required. However, as with all sampling systems, frequencies or noise above half the sample rate will be aliased and may appear in the band of interest. If this is the case, an external antialiasing filter will be required on the input. A one or two pole Butterworth low-pass filter will usually suffice. An unstable clock frequency can also produce the effect of an aliased signal. In applications where sampling residue may affect system performance, a single pole RC filter may be added to the output.

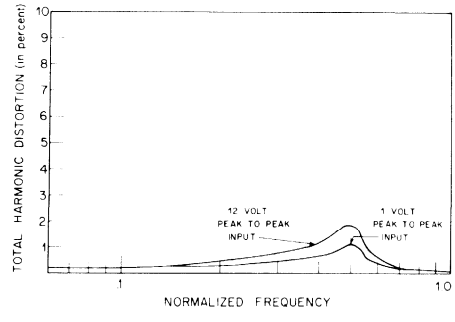


Figure 6. Typical total harmonic distortion

Table I
Absolute Maximum/Minimum Ratings * R5609/5613

	Min	Max	Units
Input Voltage-any terminal with respect to substrate[1]	-.4	21	V
Output short circuit duration-any terminal	—Indefinite—		
Input/Output current-any terminal externally forced[2]		10	mA
Power Dissipation[3]	500		mW
Storage Temperature	-55	125	°C
Operating Temperature-plastic	0	70	°C
-ceramic	-25	85	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

***Caution:** Observe MOS Handling & Operating Procedures*
**Operation at these limits may result in permanent damage.*

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{QDD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

2

Table II: Device Characteristics & Operation Range Limits[1] R5609/R5613

Parameter	Conditions & Comments	Symbol	Min	Typ	Max	Units
Supply Voltages		V_{DD}, V_{SS}	±5		±10	V
Quiescent Current[2]	No load	I_Q	9	12	16	mA
Clock Frequency	$f_c = 2 \times f_s$	f_c	1		2500	KHz
Clock Pulse Width	Ext. drive	t_c	200		$10^9/f_c$-200	nsec
Input Clock Threshold Level		V_{th}	0.8	2.2	3.0	V
Output Signal[3]	V_{in} = 14-20V p-p RL≥10KΩ	V_o	12	13.3		V_{pp}
	$R_L = 0\Omega$	I_o		4		mA
Clock to Corner	R5609	f_c/f_0	97	100	109	
Frequency Ratio Range	R5613		124	128	132	
Corner Frequency Range[3]	Max	f_0	16	20	25	KHz
	Min		10	50	100	Hz
Input Impedance		Ri		≥10		MΩ
		Ci			≤15	pF
Load Impedance(s)		R_L	≥10			KΩ
		C_L			≤50	pF
Dynamic Output Impedance	Small signal	R_o		10	250	Ω

1. $V_{DD}^{+} = +10V$, $V_{SS}^{-} = -10V$, f_c = 500 KHz, T = 25°C
2. Increase 15% for operation to 0°C.
3. Performance degrades at temperatures above 25°C.

Table III: Performance Standards[1] R5609/R5613

Parameter	Comments	Symbol	Min	Typ	Max	Units
Output Noise[1]	$BW = f_S/2$	e_n			2.5	mV_{rms}
Dynamic Range[1]	V_{Op-p}/e_n	D.R.	70	75		dB
Total Harmonic Distortion		THD		(See Fig. 6)	3	%
Insertion Loss			-.4	0	+.4	dB
Clock Feedthrough	$Bw = f_C$			30	60	mV p-p
Ripple[2]			-.2		+.2	dB
DC Offset Voltage			-0.6	0.1	+0.6	Vdc

1. Measured with ±10V supply at 25°C, $f_C = 500$ KHz, $R_L = 500K\Omega$
2. R5609 only. Not applicable for R5613.

EG&G RETICON R5611 HIGH-PASS FILTER R5612 NOTCH FILTER

Key Features

- Easy to use
- No external components required
- Small size: 8 pin mini-DIP
- Wide power supply range: ± 5V (or 10V) to ± 10 (or 20V)
- Dynamic Range: up to 80 dB
- Insertion loss: 0 dB

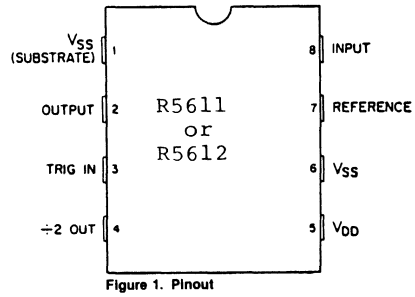


Figure 1. Pinout

Description

The Reticon R5611 and R5612 are monolithic switched-capacitor filters fabricated in Reticon's proven double-poly NMOS process.

The R5611 is a five-pole, Chebyshev high-pass filter with 30 dB per octave rolloff and less than 0.6 dB of pass-band ripple.

The Reticon R5612 is a four-pole notch filter with over 50 dB of rejection at the notch frequency.

The stability of the switched-capacitor filters eliminates alignment problems and the need for tight tolerance components and trimpots.

Typical Applications

- Antialias filters
- Reconstruction filters
- Tracking filters
- Audio analysis
- Telecommunications
- Portable instrumentation
- Biomedical/Geophysical instrumentation
- Speech processing

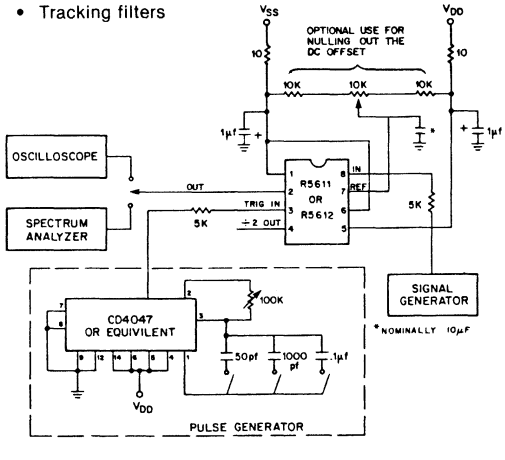


Figure 2. Test circuit

Note: the following should be applied in test and production circuits as applicable.
1) Power supply resistors may be required for transient protection.
2) Input and trigger resistors are required if signals may be applied with power off, and there is not a resistor already in series with the input.

Device Operation

The R5611 and R5612 are self-contained and require only an external clock trigger, either TTL or CMOS, and power supply. The device characteristic and operating parameters were obtained using the test configuration shown in Figure 2.

In applications where DC information is not desired through the filter, the output offset may be nulled out by varying the reference voltage, which will change the input trigger level and may require adjustment of clock voltage values. The reference input requires less than 100 µA of current and must always be well-filtered. A circuit that may be used to adjust out the output offset is shown as optional resistors in Figure 2.

A divide-by-two output is also available. This output contains a square wave at the sample rate and may be used for triggering, summing out the sample rate residue, or driving additional filters especially when filtering requirements are spaced by an octave. Gain and phase tracking from device to device (over the temperature range) is typically better than 0.5%. This measurement excludes the fixed offset of f_c/f_0 tolerance at room temperature.

Pre/Post Filtering Considerations

The typical sampling rate on the R5611 is 250 times the corner frequency and for the R5612 it is 415. (Note: Sampling rate = ½ input clock trigger rate.) Because these sample rates will be far from the frequencies of interest in most cases, antialiasing filtering will usually not be required. However, as with all sampling systems, frequencies or noise above half the sample rate will be aliased and may appear in the band of interest. If this is the case, an external antialiasing filter will be required on the input. A one or two pole Butterworth low-pass filter will usually suffice. An unstable clock frequency can also produce the effect of an aliased signal. In applications where sampling residue may affect system performance, a single pole RC filter may be added to the output.

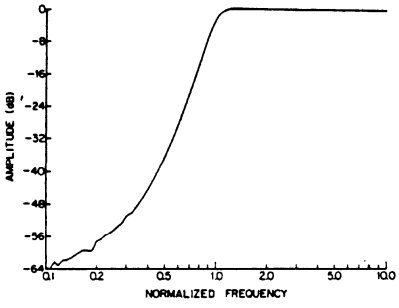


Figure 3. Frequency response of R5611 high-pass filter.

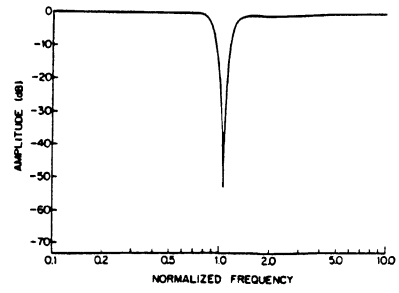


Figure 4. Frequency response of R5612 notch filter.

Table I
Absolute Maximum/Minimum Ratings*

	Min	Max	Units
Input Voltage-any terminal with respect to substrate[1]	-.4	21	V
Output short circuit duration-any terminal	—Indefinite—		
Input/Output current-any terminal externally forced[2]		10	mA
Power Dissipation[3]	500		mW
Storage Temperature	-55	125	°C
Operating Temperature	0	70	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

Caution: *Observe MOS Handling & Operating Procedures*
**Operation at these limits may result in permanent damage.*

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{QDD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

Table II: Device Characteristics & Operation Range Limits[1]

Parameter	Conditions & Comments	Symbol	Min	Typ	Max	Units
Supply Voltages		V_{DD}, V_{SS}	±-15		±10	V
Quiescent Current[2]	No load	I_Q	9	12	16	mA
Clock Frequency	$f_c = 2 \times f_s$	f_c	1		2500	KHz
Clock Pulse Width	Ext. drive	t_c	200		$10^6/f_c$-200	nsec
Input Clock Threshold Level		V_{th}	0.8	2.2	3.0	V
Output Signal[3]	V_{in} = 14-20V p-p RL≥10KΩ $R_L = 0\Omega$	V_o I_o	12	13.3 4		V_{pp} mA
Clock to Corner	R5611	fc/f_0	485	500	515	
Frequency Ratio Range[3]	R5612		900	930	960	
Corner Frequency	R5611	f_0	10		8000	
Range[3]	R5612		10		5000	Hz
Input Impedance		Ri Ci		≥10	≤15	MΩ pF
Load Impedance(s)		R_L C_L	≥10		≤50	KΩ pF
Dynamic Output Impedance	Small signal	R_o		10	250	Ω

1. $V_{DD}^{+} = +10V$, $V_{SS}^{-} = -10V$, f_c = 500 KHz, T = 25°C
2. Increase 15% for operation to 0°C.
3. Performance degrades at temperatures above 25°C.

Table III: Performance Standards[1] R5609/R5613

Parameter	Comments	Symbol	Min	Typ	Max	Units
Output Noise[1] R5611 R5612	BW = $f_s/2$	e_n			1.0 1.5	mV_{rms}
Dynamic Range[1]	V_{Op-p}/e_n	D.R.		80		dB
Total Harmonic Distortion		THD			0.3	
Insertion Loss			-0.4	0	+0.4	dB
Clock Feedthrough	Bw = f_c			30	60	mV p-p
Notch-Q (R5612)			2.9	3.0	3.1	
Notch Rejection (R5612)			50	55		dB
Pass-band Ripple R5611 R5612					0.6 0.2	dB dB
Output DC Offset			-0.6	0.1	0.6	Vdc

1. Measured with ±10V supply at 25°C, f_c = 500 KHz, R_L = 500KΩ

R5614 1/3 OCTAVE BANDPASS FILTERS
R5615 1/2 OCTAVE BANDPASS FILTERS
R5616 FULL OCTAVE BANDPASS FILTERS

Description

The Reticon R5614, R5615, and R5616 are monolithic switched-capacitor band-pass filters packaged in 8-pin mini-DIP's.Each contains a 6-pole Chebyshev ANSI Class II band-pass filter using one external input clock trigger.

The center frequency of the filters is tunable by the clock frequency to greater than 20 KHz. The dynamic range is better than 86 dB and distortion can be less than 0.1%. The filters will handle input signals of greater than 17 volts p-p with an insertion loss of less than ±0.2 dB.

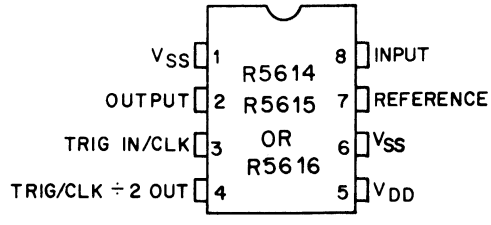


Figure 1. Pinout.

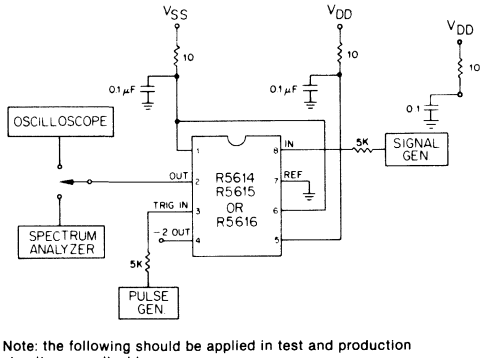
Device Operation

The band-pass filters are self-contained and require only an external clock trigger and plus and minus power supplies to operate. The device characteristics and operating parameters were using the test configuration shown in Figure 2.

Typical Applications

- Spectrum analysis (parallel or swept filters)
- Audio filtering
- Noise analysis
- Equalization
- Harmonic analysis

An equivalent inductor-capacitor (LC) circuit (Figure 3) is transformed into a leap-frog configuration (Figure 4) for use in the integrated circuit. The building blocks used in the leap-frog schematic are realized using switched-capacitor integrators (see Figure 5).



Note: the following should be applied in test and production circuits as applicable.
1) Power supply resistors may be required for transient protection.
2) Input and trigger resistors are required if signals may be applied with power off, and there is not a resistor already in in series with the input.

Figure 2. Test Circuit for R5614, R5615, and R5616.

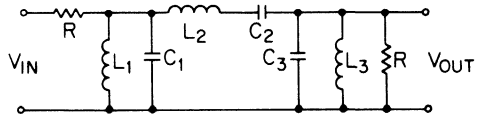


Figure 3. L-C circuit equivalent to the switched capacitor filter.

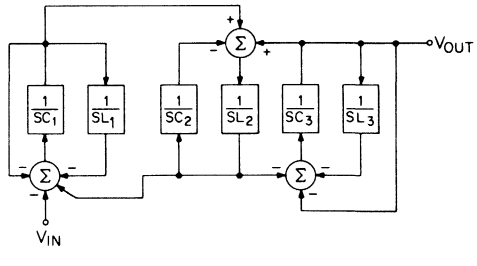


Figure 4. Filter realization-Active leap-frog technique.

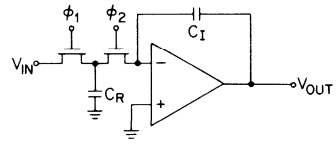


Figure 5. Switched capacitor resistor integrator used in the leap-frog filter realization.

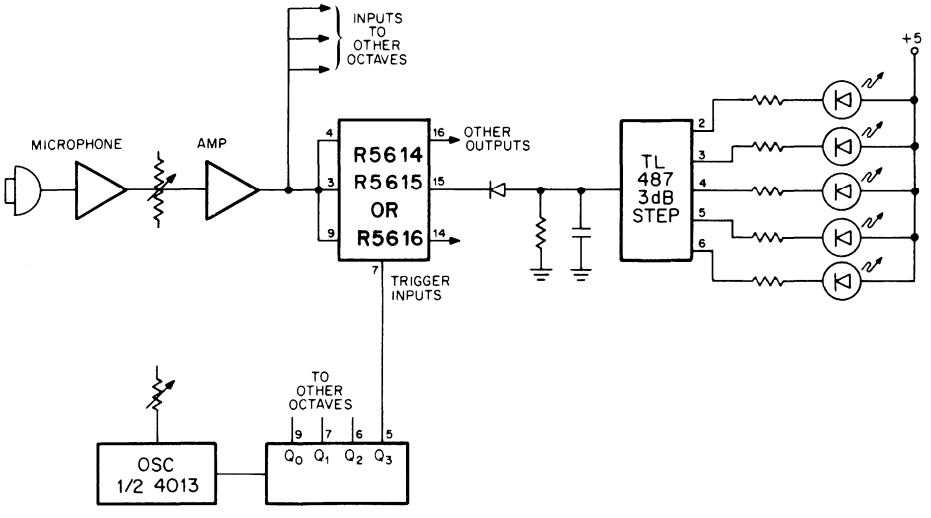


Figure 6. Typical application-Audio spectrum analyzer.

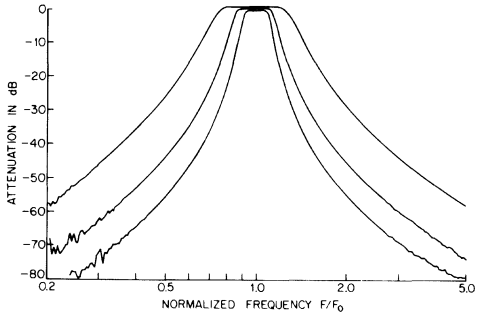


Figure 7 Normalized frequency response for R5614, R5615 and R5616.

Antialiasing Considerations

The sampling rate on the ANSI filters is approximately 27 times the filter center frequency. As in all sampled data systems, signals above half the sampling frequency (fs) will be aliased and may appear in the band of interest. If signals greater than 13.5 fo will be applied to the filter, an external antialiasing filter may be required. In applications where the clock residue may affect system performance, a single pole filter should be added to the filter output. Typical clock residue is 25 mV p-p.

Note that the input trigger clock frequency, f_C, is twice the sample rate, or approximately 54 times the center frequency. The input clock rate is divided by two in generating the on-chip clock waveforms which control the sample rate, fs.

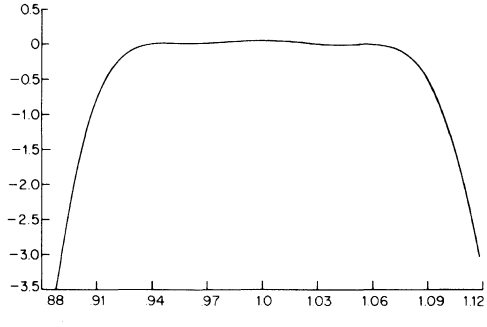


Figure 8. Expanded Pass-band response curve for R5614.

Table I
Absolute Maximum/Minimum Ratings*

	Min	Max	Units
Input Voltage-any terminal with respect to substrate[1]	-.4	21	V
Output short circuit duration-any terminal	—Indefinite—		
Input/Output current-any terminal externally forced[2]		10	mA
Power Dissipation[3]	500		mW
Storage Temperature-plastic	-55	125	°C
Operating Temperature-plastic	0	70	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

Caution: *Observe MOS Handling & Operating Procedures*
**Operation at these limits may result in permanent damage.*

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{ODD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

2

Table II
Device Characteristics

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Input Impedance	Ri	3			Megohms
Input Capacitance	Ci			20	pF
Dynamic Output Impedance	Ro			10	ohms
Maximum Output Capacitive Load		50			pF
Trigger Clock Input Capacitance	C_C			10	pF
Positive Supply	V+	5		10	volts
Negative Supply	V-	-5		-10	volts
Clock Trigger[1] [2] Voltage	Vc	2.2		V+	volts
Trigger Pulse Width	Tcp	200		tc-200	nS
Center Frequency	fc	0.5		20,000	Hz

Table III
Performance Specifications*

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Clock to Center Frequency Ratio	fc/fo (= 2 x fs/fo)	52	54.5	57	
Q: R5614 R5615 R5616		4.50	4.70 3.00 1.48	4.80	
Supply Current	I_D		8		mA
Maximum Output Current	Io	2			mA
Output Voltage Swing	Vo		17		volts p-p
Output Noise[2]			0.35	0.4	mV_{rms}
Dynamic Range[3]			86	95	dB
Total Harmonic Distortion[3] @ 2 KHz 17Vp-p 2Vp-p				0.5 0.1	%
Power Supply Rejection V+ (to 50 KHz) Subt V- (20 KHz/50 KHz			40 30/25		dB
Insertion Loss		-0.2	0	0.2	dB
Pass-band Ripple			.20	.50	dB

1. All devices are internally gate protected for static immunity. Applying AC signals or clock to chip with power off may exceed negative limit.
2. Trigger voltage is CMOS/TTL.
3. Broad band to 1/2 the sample rate.
4. V = ± 10V, fo = 2KHz

*V+ = 10V V− = −10 v F_O = 2 KHz 25°C

Table IV
ANSI Specifications for Typical 3 dB Bandwidth and Minimum 40 dB Rolloff

		3 dB Bandwidths		40 dB Bandwidths	
	FO	LOW	HIGH	LOW	HIGH
Third Octave Filter	1	0.89	1.11	0.64	1.52
Half Octave Filter	1	0.62	1.19	0.51	1.96
Full Octave Filter	1	0.72	1.40	0.31	3.29

Analog Signal Processing Products

DESCRIPTION

The R5630 and R5631 are monolithic IC filters now available for use in the band separation filtering of low speed (300 baud) originate/answer modem applications.

The devices contain two 10-pole switched-capacitor bandpass filters fabricated in NMOS technology and are packaged in a single 16 pin dip. (Pin-out diagram shown in Figure 2.)

These transmit and receive filters are compatible with 103/113 (R5630) and CCITT V.21 (R5631) modems. Switching the filters between originate and answer modes is accomplished by an external TTL compatible input pin.

Included on the chip is a receive gain control stage externally adjustable from 0 to 30 dB, a separate limiter for use with the receive output, a TTL compatible input for self-test mode, and an on-chip oscillator. The block diagram of the R5630/R5631 is shown in Figure 1.

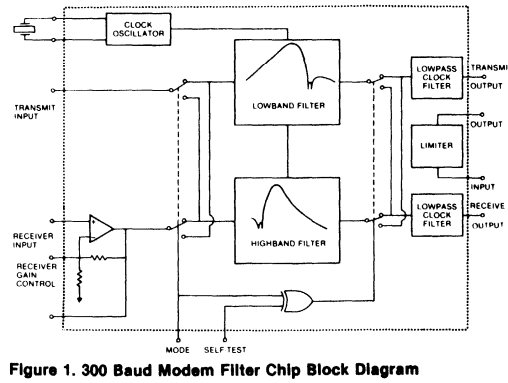


Figure 1. 300 Baud Modem Filter Chip Block Diagram

3

DEVICE OPERATION

The modem filters are self-contained, and to operate, they require only plus and minus supplies and either an external TTL (or CMOS) 1 MHz input clock, or a 1 MHz crystal, with two capacitors and a resistor (as shown in Figure 3). With accurate clocking, center frequency shifts of the filters are less than ±1%. For either the highband or lowband filter, maximum S/N is obtained when the input, after the mode switches, is 6 V p-p for ±5V only (12V p-p for ±10V supplies). For optimum receive performance at minimum S/N (=6-10 dB), the circuitry of Fig. 4 is recommended. Then low level signals will be limited by the Output Noise specification.

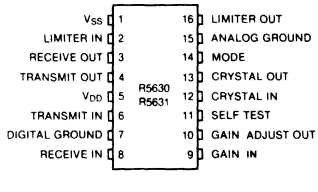


Figure 2. Pin Assignment R5630/R5631

GAIN ADJUST

For tight control of receive gain, it is recommended that an attenuation network, such as a resistor divider, be placed ahead of the receiver input. The device has a receive gain of 18.5 dB ±1 dB. Note that gain control, pins 9 and 10, is also accomplished by the parallel resistor technique; however, device to device variation restricts tight gain control from these pins unless resistor values are selectable or a trimpot is used. Refer to Figure 9 for further information.

LIMITER OPERATION

It is recommended that an AC coupled lowpass filter be placed between the R_X Output and the Limiter Input. Component values are chosen based on the limiter input impedance. In this way, the filter D.C. offset is blocked and limiter operation is constrained to the signal bandwidth. The bandwidth consideration is important; typically 5-20 mV p-p of clock feedthrough, oscillator/sampling frequency(s), is inherent in SCF's. Note also the potentiometer for compensation of the Limiter Offset Voltage. The component value can be chosen between 100 KΩ and 1 MΩ. Either Offsets or clock feedthrough raise the apparent Output Noise and reduce the Dynamic Range.

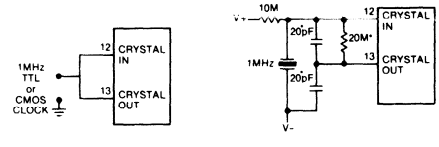


Figure 3. Clocking Circuits

*Component values may vary with parasitic capacitances.

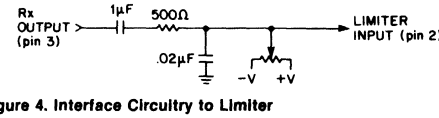


Figure 4. Interface Circuitry to Limiter

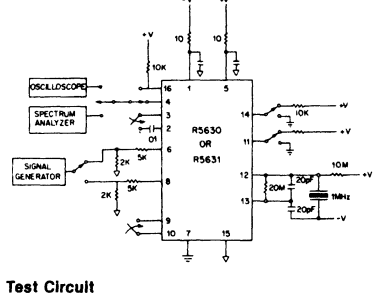


Figure 5. Test Circuit

TABLE I. ABSOLUTE MAXIMUM/MINIMUM RATINGS

	Min	Max	Units
Input Voltage-any terminal with respect to substrate (1)	−.4	21	V
Output short circuit duration-any terminal	Indefinite		
Input/Output current-any terminal (externally forced)		10	mA
Power Dissipation (2)	500		mW
Storage Temperature-plastic	−55	125	°C
Operating Temperature-plastic	0	70	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

CAUTION: Observe MOS Handling & Operating Procedures

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{QDD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

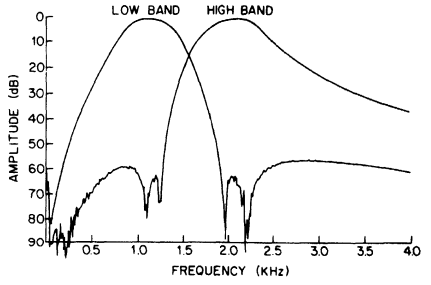


Figure 6. Frequency Response of R5630, 300 Baud Modem Filter

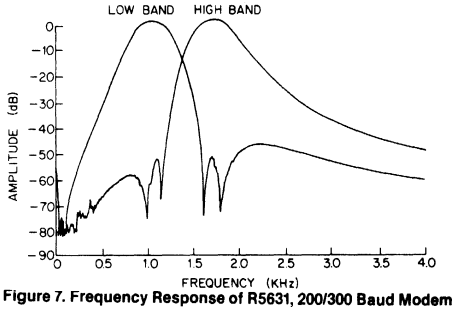


Figure 7. Frequency Response of R5631, 200/300 Baud Modem Filter

TABLE II. DEVICE CHARACTERISTICS & OPERATION RANGE LIMITS (1)

PARAMETER*	CONDITIONS & COMMENTS	SYMBOL	MIN	TYP	MAX	UNITS
Input Bias Current	Typ @ 25°C Max @ 70°C	I_B		.001-.01	10	nA
Input Impedance(s)		R_i	>10			MΩ
		C_i			10	pF
	Limiter Only	R_i		3		KΩ
	Limiter Only	C_i		100		pF
Load Impedance(s)		R_L-Tx	.6	27		KΩ
		R_L-Rx	10	27		KΩ
		R_L-Lim.Out.	2.7	10		KΩ
		C_L-Tx			5000	pF
		C_L-Rx			1000	pF
Output Impedance	Small-signal	R_O-Tx		2	10	Ω
	Small-signal	R_O-Rx		10	100	Ω
Output Offset Voltage(s)	Tx & Rx	V_{off}		20-50	200	mV
Limiter Offset Voltage	input			5		mV
Output Signal	V_i = 6-10V p-p, R_L = 600Ω	V_O-Tx	2.2		3.0	V p-p
	V_i = 6-10V p-p, $R_L \geq$ 27KΩ	V_O-Tx, Rx	4.8	5.5	6.2	V p-p
	V_i = 6-10V p-p, R_L = gnd	I_O-Tx			10	mA
	V_i = 6-10V p-p, R_L = gnd	I_O-Tx			2	mA
	Input ≥ +15mV, $R_{LIM} \geq$ 2.7KΩ	V_{LIM}-Low	.4	.6	.8	V
Digital Input Threshold levels (Mode, Self-Test, Clock)		V_{TH}	.8	1	1.3	V
Mark/Space (5630) Frequency	Highband	f_{0H}		2125		Hz
	Lowband	f_{0L}		1170		Hz
(5631)	Highband	f_{0H}		1750		Hz
	Lowband	f_{0L}		1080		Hz
Clock Frequency	$f_c = 2 f_s$	f_c		1		MHz
Clock Pulse Width	Ext. drive	τ_c	200		$10^9/f_c$-200	nS
Supply Voltages		V_{DD}+	4	5	10.5	V
		V_{SS}-	-4	-5	-10.5	V
Quiescent Current (2)	No load	I_{QDD}	10	12	20	mA
		I_{QSS}	11	13	20	mA

(1). V_{DD}+ = 5V, V_{SS}- = -5V, f_s = 250 KHz (i.e., f_c = 1 MHz), 25°C **(2).** Increase 15% for operation at 0°C
Increase 30% for operation at ± 10V

TABLE III. PERFORMANCE STANDARDS (4)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
R5630 & R5631					
Output Noise (1)			1.0	2.0	mV_{rms}
Dynamic Range (2)	D.R.	67	72		dB
Total Harmonic Distortion (2)					
@ f_O = 1 KHz	THD Low Band		0.5	.5	%
	THD High Band		1.0	2.0	%
Crosstalk			-60	-62	dB
Insertion Loss		0	1	2	dB
Ripple (2)			1	2	dB
R5630 only-					
3dB Band width Low Band	BW Low Band	435	460	485	Hz
High Band	BW High Band	475	520	545	Hz
Adjacent Channel Rejection LB		57	58	60	dB
HB		59	60	62	
Group Delay Variation (3)	G.D.		50	100	μsec
R5631 only-					
3dB Band width (Both Bands)	BW	330	350	370	Hz
Adjacent Channel Rejection		50	53	55	dB
Group Delay Variation (3)		80	100	120	μsec

(1). Broad band to 1/2 the sample rate (fs). Measured with circuit similar to Fig. 4.

(2). 5 volts p-p input. (D.R. = pp output divided by rms noise).

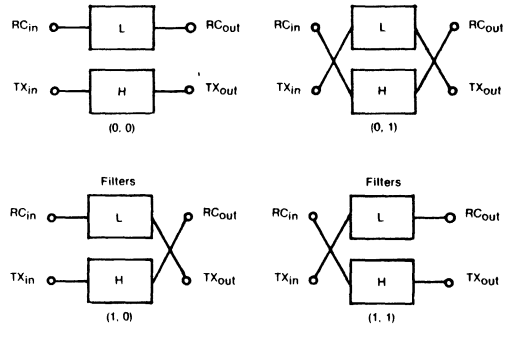
(3). G.D. = $\Delta\phi/\Delta f$, Δf = Mark to Space frequencies, $\Delta\phi$ = relative phase shift in radians between mark and space frequencies.

(4). V + = 5V, V − = −5V, f_C = 1 MHz, 25°C, f_S = 250 KHz, R_L >27KΩ

TABLE IV. OPERATIONAL PROGRAMMING

SELF TEST	MODE	RC.IN	RC.OUT	XMIT.IN	XMIT. OUT
0	0	L	L	H	H
0	1	H	H	L	L
1	0	L	H	H	L
1	1	H	L	L	H

L = Lowband Filter
H = Highband Filter



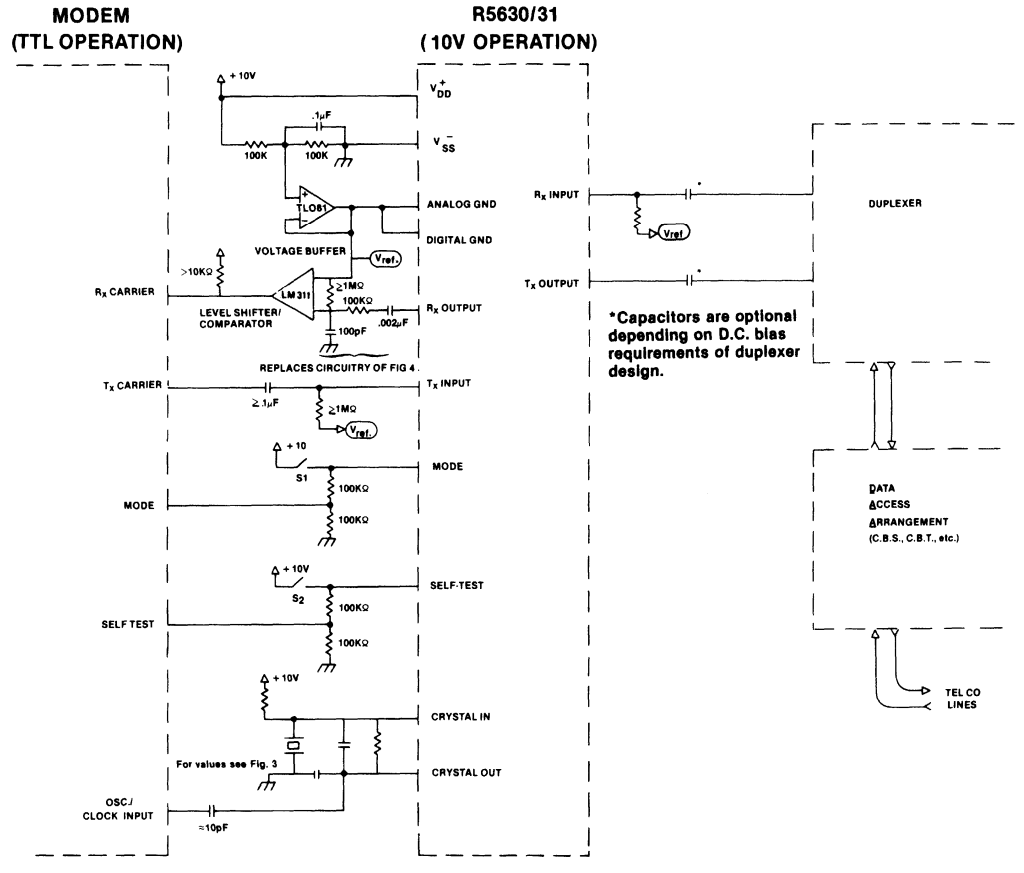


Figure 8. Single Supply Operation

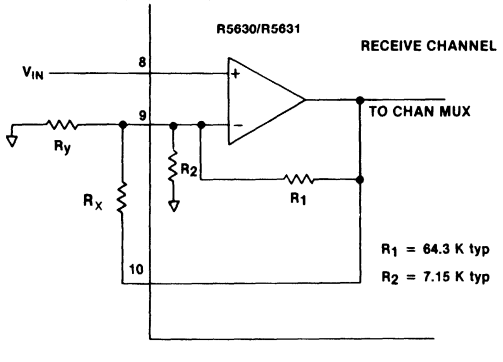


Figure 9. Gain Adjust Schematic

Both R_1 and R_2 are implemented as polysilicon resistors. For the "worst-case" calculations, variance of their value ought to be set at ±40%. If the parallel combination of R_1 and R_X ($R_1//R_X$) is represented by R_f, and R_2 and R_Y ($R_2//R_Y$) by R_S, then the gain equation is simplified:

$$20 \log (R_f/R_S) = \text{Gain (db)}$$

From this a gain tolerance can be evaluated. Note that the value of R_1 and R_2 change from typical by the same percentage, plus or minus. For example, when Ry is 6.8KΩ and Rx is 18KΩ, the gain is 12dB ± 1dB.

Gains to 30 dB are possible if care is taken such that the loading of the on-chip op-amp does not fall below 10KΩ.

General Description

The Reticon R5632 is a monolithic switched capacitor filter network designed for use in full duplex Bell 212A and CCITT V.22 1200 baud modem filtering applications. The device contains two channels of band-pass filters, fabricated using an industry standard double-poly NMOS process. Each channel consists of a ten pole band-pass filter and a ten pole all-pass section. These provide compensation for filter and delay line distortions in the passband to improve data transmission quality. Each channel is provided with an uncommitted operational amplifier which can be used as a gain amplifier, antialiasing filter, or clock residue filter. The band-pass filters are centered at 1200 Hz (low band) and 2400 Hz (high band). For CCITT V.22 applications, a select pin is provided for switching in either the 550 Hz or 1800 Hz guard tone notch filter.

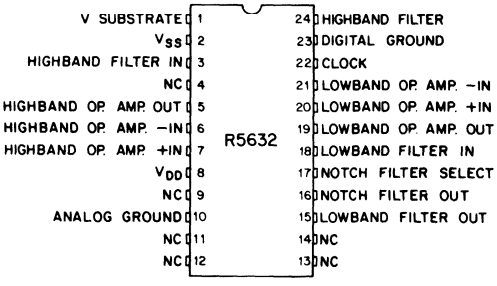


Figure 1. Pin Out.

3

Key Features

- **Bell 212A compatible filters with full channel compromise equalization in *both* bands.**
- **Switchable CCITT V.22 compatible low band guard tone notches at 550 Hz and 1800 Hz.**
- **Suitable for Bell 103/113 configurations.**
- ***Less* than ±100 μsec group delay slope variation.**
- ***Greater* than 55 dB of adjacent channel rejection.**
- **Two on-chip uncommitted operational amplifiers for user designated functions.**
- **Industry proven NMOS switched capacitor technology.**
- **±4V to ±11V power supply range.**
- **Up to 950 Hz bandwidth.**
- **±1% Center Frequency accuracy.**
- **TTL/CMOS compatible digital inputs.**

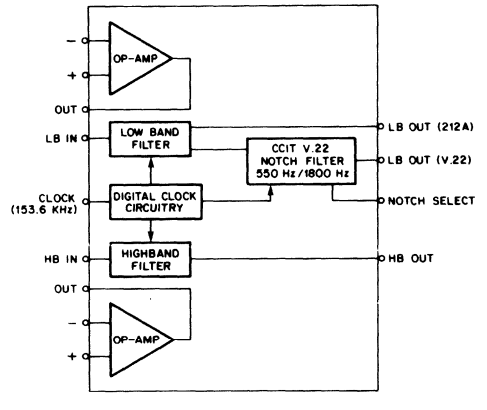


Figure 2. Functional Block Diagram, R5632.

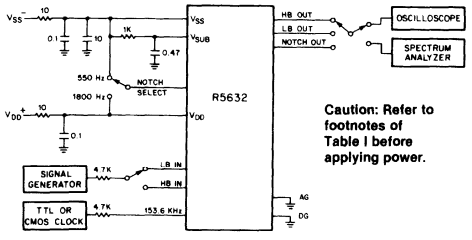
Device Operation

The functional block diagram of the R5632 is shown in Figure 2. The basic function blocks are the low band filter, high band filter, guard tone notch filters, and two uncommitted operational amplifiers. Each band includes full channel delay and filter equalization for optimum "eye pattern" performance. The amplitude response and group delay of the low band filter are shown in Figures 4 and 5, respectively. These plots are representative of the Bell 212A characteristics. Note, also, that these characteristics are virtually unchanged in the R5632 when either the 550 Hz or 1800 Hz CCITT Guard Tone notch filters are chosen via the NOTCH SELECT pin, (see Figures 7a, 7b; 8a, 8b).The low band filter includes full-channel compromise equalization.

For the high band filter, the amplitude response and group delay are shown in Figures 4 and 6. The response has a slight positive slope to compensate for typical Bell specified line conditions. Note that for both the low band and high band, the group delay slope variation is a maximum of ±100 μseconds. The unweighted adjacent channel rejection is greater than 55 dB.

The R5632 is operated with an external 153.6 KHz clock, which can be TTL or CMOS. This clock is the standard frequency of the Bell 212A system. Since the filters are clock tunable, any variation in the clock accuracy will add to the device-to-device center frequency tolerance. With accurate clocking, center frequency shifts of the filters are less than ±1%. This tunability can be used to an advantage if a different center frequency is desired along with a proportionately scaled bandwidth.

The R5632 can operate over a wide power supply voltage range, ±4V to ±11V maximum. This voltage range can be a split supply or a single supply (+22V maximum) with an AC ground at halfway between the voltage spread. For either the low band or high band filter, maximum S/N is obtained when the input is 5V p-p for ±5V supplies (12V p-p for ±10V supplies). For particularly noisy switcher power supplies, it may be necessary to provide power supply and substrate filtering as shown in the test circuit (Figure 3).



Caution: Refer to footnotes of Table I before applying power.

Figure 3. Test Circuit.

TABLE I: ABSOLUTE MAXIMUM/MINIMUM RATINGS

	Min	Max	Units
Input Voltage—any terminal with respect to substrate(1)	-.4	22	V
Output short circuit duration—any terminal		Indefinite	
Input/Output current—any terminal (externally forced)(2)		10	mA
Power Dissipation(3)	500		mW
Storage Temperature—plastic	-55	125	°C
—ceramic	-55	150	
Operating Temperature—plastic	0	70	°C
—ceramic	-40	85 °C	
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

CAUTION: Observe MOS Handling & Operating Procedures

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{QDD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

TABLE II
DEVICE CHARACTERISTICS & OPERATION RANGE LIMITS(1,2)

Parameter	Symbol	Conditions & Comments	Min	Typ	Max	Units
Supply Voltages	V_{DD} +		5		10	V
	V_{SS}-		5		10	V
Quiescent Current	I_Q	(No load)				
		±5V	8	11	17	mA
		±10V	12	16	25	mA
Clock Frequency	fc			153.6		KHz
Clock Pulse Width	τc		200	sq. wave	$10^9/f_C$-200	nsec
Input Clock Threshold Level			0.8	1.1	1.6	V
Output Signal	V_O	±5V			5	V p-p
		±10V (R_L = 27KΩ)			12	V p-p
Input Bias Current	I_B			.001-.01	10	nA
Input Impedance(s)		Ri	10			MΩ
		Ci			10	pF
Load Impedance(s)	R_{LL}	Low band	10	27		KΩ
	C_{LL}		50	100		pF
	R_{HL}	High band	0.6	27		KΩ
	C_{HL}	or Notch	500	1000		pF
Center Frequency	f_0	Low band	1188	1200	1212	Hz
		High band	2376	2400	2424	Hz
Dynamic Output Impedance	R_O	Low band			100	Ω
		High band			10	Ω

(1) Data applies to both bands unless otherwise noted.

(2) V_{DD} = + 10V, V_{SS} = − 10V, fc = 153.6 KHz, 25°C.

TABLE III
PERFORMANCE STANDARDS R5632 (1,2)

Parameter	Symbol	Conditions & Comments	Min	Typ	Max	Units
Maximum Output Noise				1	2	mV rms
Crosstalk			65	70		dB
Total Harmonic Distortion	THD			0.3	0.6	%
Dynamic Range	D.R.			70		dB
3 dB Bandwidth	BW		900		950	Hz
Adjacent Channel Rejection-Low band			65			dB
-High band			75	85		dB
Average Group Delay Slop (over passband)-Low band	G.D.		+180	280	+380	μsec
-High band			-400	-300	-200	μsec
Power Supply Ripple Rejection $-V_{DD}$		In passband.	0	15		dB
		From 4 KHz to 50 KHz.	15			dB
$-V_{SS}$		In passband.	0	18		dB
		From 4 KHz to 50 KHz.	15			dB
Passband Gain at Center Frequency			-1.5	-0.5	0.5	dB
Stop Band Rejection-Low band		@2400 Hz	65	85		dB
		@1900 Hz	50			dB
		@1800 Hz	25			dB
		@1800 Hz, ±2Hz (V.22)	44			dB
		@550 Hz, ±2Hz (V.22)	44			dB
-High band		@1200 Hz	75	85		dB
		@1700 Hz	40			dB
		@4000 Hz	30			dB
		below 550 Hz	50			dB
Group Delay in Passband-Low band		@ 900 Hz	4960	5060	5160	μsec
		@1000 Hz	5140	5240	5340	μsec
		@1200 Hz	5230	5330	5430	μsec
		@1400 Hz	5260	5360	5460	μsec
		@1500 Hz	5220	5320	5420	μsec
-High band		@2100 Hz	4820	4920	5020	μsec
		@2200 Hz	5050	5150	5250	μsec
		@2400 Hz	5020	5120	5220	μsec
		@2600 Hz	4950	5050	5150	μsec
		@2700 Hz	4880	4980	5080	μsec

(1) Data applies to both bands unless otherwise noted.
(2) V_{DD} = +10V, V_{SS} = −10V, fc = 153.6 KHz, 25°C

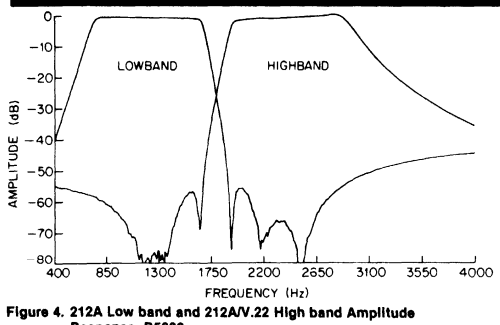


Figure 4. 212A Low band and 212A/V.22 High band Amplitude Response, R5632.

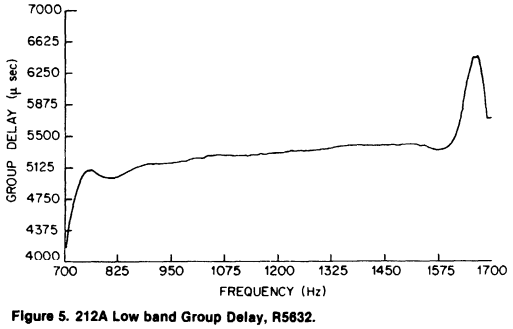


Figure 5. 212A Low band Group Delay, R5632.

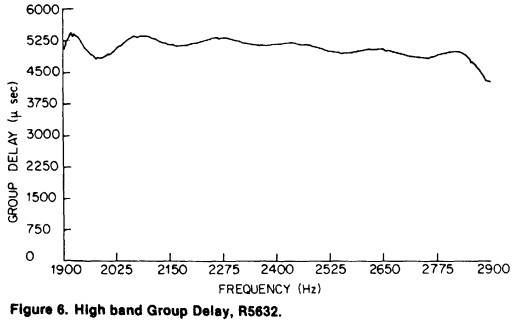


Figure 6. High band Group Delay, R5632.

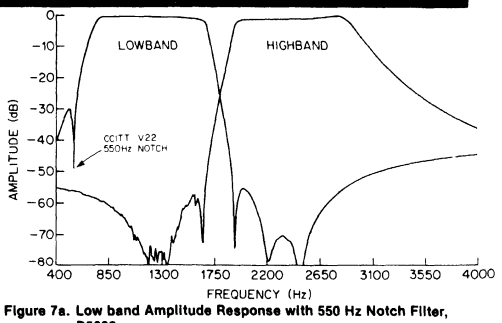


Figure 7a. Low band Amplitude Response with 550 Hz Notch Filter, R5632.

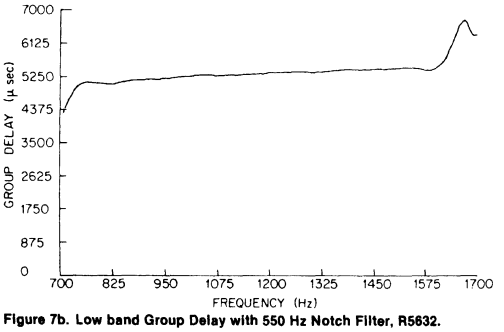


Figure 7b. Low band Group Delay with 550 Hz Notch Filter, R5632.

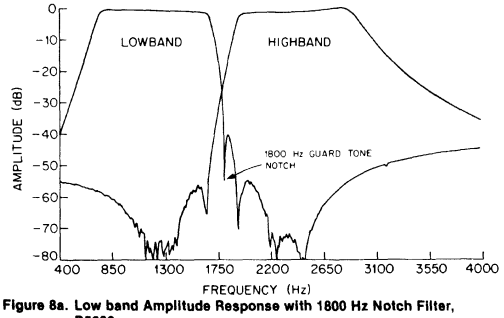


Figure 8a. Low band Amplitude Response with 1800 Hz Notch Filter, R5632.

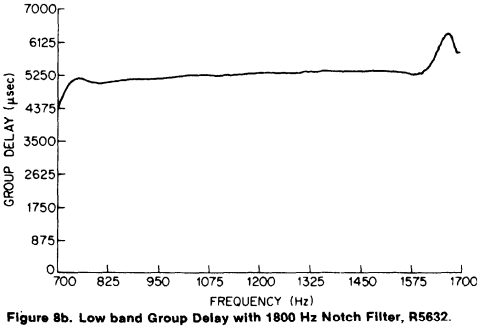


Figure 8b. Low band Group Delay with 1800 Hz Notch Filter, R5632.

The Reticon R5633 is a switched-capacitor bandpass filter bank and multiplexer designed for low speed modem and DTMF applications. The chip contains 3 bandpass filters which, depending on the input clock rates and multiplexer configuration, may be used for 103, V21, and videotext modem filters and DTMF band split filters.

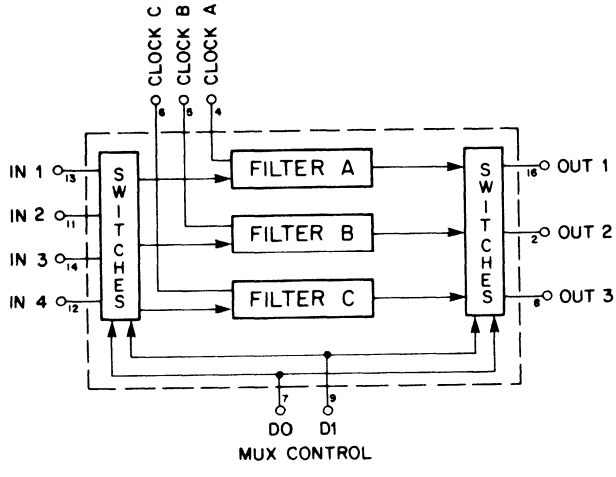


Fig 1. Block Diagram

The multiplexer is set up so that switching between answer and originate modes for 103 and V21 modem filters can be accomplished with one of the multiplexer inputs. The functional block diagram is shown in Figure 1, the pin out in Figure 2, and the test circuit in Figure 3. In the test circuit, several 5KΩ resistors were used to limit current in the event that signals were applied without supply voltages biasing the chip. Filter A is a 1/3 octave, 6-pole bandpass. Filters B and C are 5/8 octave, 6-pole bandpasses. Operation for each of the four modes is listed in Table IV. The clock rates for all of the filter configurations can be derived from either a 4 MHz or a 3.58 MHz master clock. The necessary divide by ratio's appear in parenthesis; the upper number are those for the 4 MHz crystals, the lower for 3.58 MHz. The filter connections for the various multiplexing configurations are listed in Table V.

PRELIMINARY

EG&G RETICON • 345 POTRERO AVENUE • SUNNYVALE, CALIFORNIA 94086-9930
(408) 738-4266 • TWX: 910-339-9343

TABLE I: ABSOLUTE MAXIMUM/MINIMUM RATINGS

	Min	Max	Units
Input Voltage - any terminal with respect to substrate (1)	-.4	21	V
Output short circuit duration - any terminal	Indefinite		
Input/Output current - any terminal (externally forced)		10	mA
Power Dissipation (2)	500		mW
Storage Temperature - plastic	-55	125	°C
Operating Temperature - plastic	0	70	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

CAUTION: Observe MOS Handling & Operating Procedures

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{ODD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

TABLE II: DEVICE CHARACTERISTICS & OPERATION RANGE LIMITS (1)

PARAMETER	CONDITIONS & COMMENTS	SYMBOL	MIN	TYP	MAX	UNITS
Input Bias Current	Typ @ 25°C Max @ 70°C	I_B		.001-.01	10	nA
Input Impedance(s)		R_i	>10			MΩ
		C_i			10	pF
Load Impedance(s)		R_L	.6	27		KΩ
		C_L			50	pF
Output Impedance	Small-signal	R_0		2-5	20	Ω
Output Offset Voltage(s)	T_X & R_X	V_{off}		20-50	200	mV
Output Signal	R_L = 600Ω	V_o	3.8	4	4.2	V p-p
	$R_L \geq$ 27KΩ	V_o	5.6	5.8	6	V p-p
	V_i = 6-10V p-p R_L = gnd	I_o			10	mA
Digital Input Threshold levels (Mux Control, Clock)		V_{TH}	.8	2.3	3	V
Center Frequency(s)	Filter A	f_0	10	See Table V	13.3×10^3	Hz
	Filter B	f_0	6		7.3×10^3	Hz
	Filter C	f_0	4		5.1×10^3	Hz
Clock Frequency		f_c	.001	≤1	1.25-1.5 (3)	MHz
Clock Pulse Width	Ext. drive	tc	200		$10^9/f_c$-200	nS
Supply Voltages		V_{DD}^+	5		10	V
		V_{SS}^-	-5		-10	V
Quiescent Current (2)	No load	I_{QDD}, I_{QSS}	15	19	23	mA

(1) V_{DD}^+ = 5V, V_{SS}^- = -5V, 25°C
(2) Increase 15% for operation to 0°C
Increase 30% for operation at +10V
(3) Between 1.25 and 1.5 MHz ripple increases above maximum limit

TABLE III: PERFORMANCE STANDARDS (1)

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Clock to Center Frequency Ratio	fc/fo (=2x fs/fo)				
Filter A		93	95	97	
Filter B		170	173	176	
Filter C		245	251	257	
Q:					
Filter A		3.6	4.0	4.4	
Filter B		2.1	2.3	2.6	
Filter C		2.1	2.3	2.6	
Output Noise (2)			1	3	mV_{rms}
Dynamic Range (3)		65	75		dB
Total Harmonic Distortion (3) @ 1 KHz			0.1	.4	%
Crosstalk			-60		dB
Insertion Loss		-0.5	+0.2	+0.5	dB
Pass Band Ripple A			1.0		dB
B			.2		
C			.5		

(1) V+ = 5V V- = -5V 25°C

(2) Broad band to 1/2 the sample rate. Clock feedthrough (typ. 5-20 mVp-p) filtered.

(3) 6 volts p-p input.

TABLE IV: TYPICAL FREQUENCIES

	Mux Address D_0	Mux Address D_1	Filter A	Filter B	Filter C
DTMF Bandsplit	0	0	Not Used	f_o = 1450 BW = 600 CLK = 250K (÷16) 255.6K (÷14)	f_o = 810 BW = 340 CLK = 200K (÷20) 198.8 (÷18)
Videotext	0	1	f_o = 440 BW = 110 CLK = 41.667K (÷96) 41.62K (÷86)	f_o = 1700 BW = 1300 (1) CLK = 333K (÷12) = 325.4K (÷11)	
103 Modem Originate	1	0	f_o = 2125 BW = 520 CLK = 200K (÷20) 198.8K (÷18)	f_o = 1170 BW = 485 CLK = 200K (÷20) 198.8K (÷18)	Not Used
Answer	1	1			
V21 Modem Originate	1	0	f_o = 1750 BW = 430 CLK = 166.7K (÷24) 162.7K (÷22)	f_o = 1080 BW = 435 CLK = 181.8K (÷22) 179K (÷20)	Not Used
Answer	1	1			

(1) Filters B and C are internally summed on chip producing a bandpass filter from 1100 Hz to 2400 Hz. This summing produces a 6 dB insertion loss and is configured as a high impedance node.

TABLE V: Filter Connection Programming, R5633

MUX ADDRESS D0	MUX ADDRESS D1	FILTER A	FILTER B	FILTER C
0	0	In 2, Out 2	In 1, Out 1	In 1, Out 3
1	0	In 2, Out 2	In 1, Out 1	In 1, Out 3
0	1	In 1, Out 1	In 4, Out 2*	In 3, Out 2*
1	1	In 1, Out 1	In 2, Out 2	N/C
		* Filters B & C output summed		

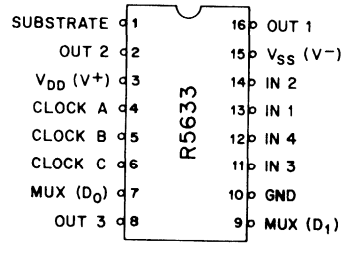


Fig. 2 Pin Configuration

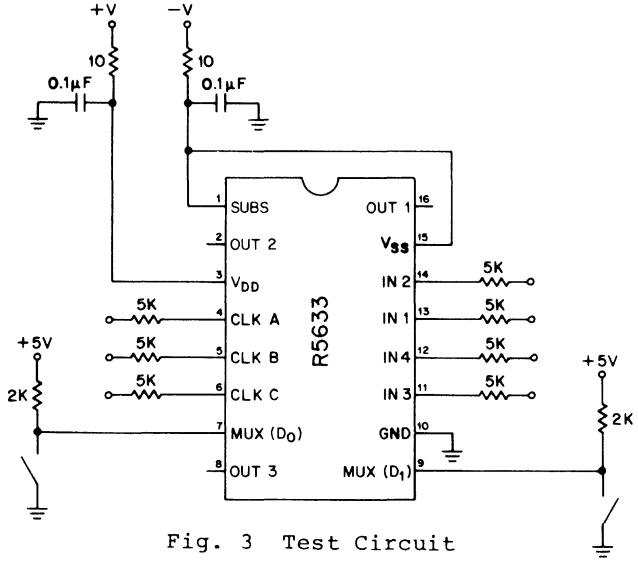


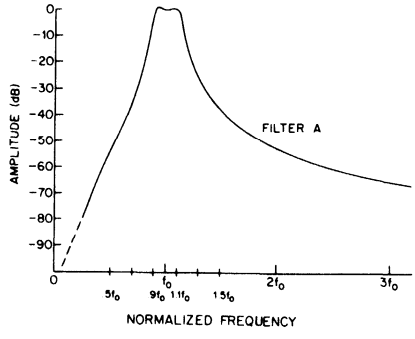
Fig. 3 Test Circuit

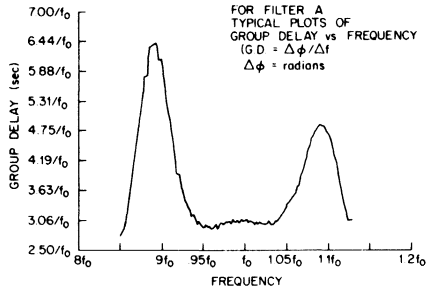
NOTE:

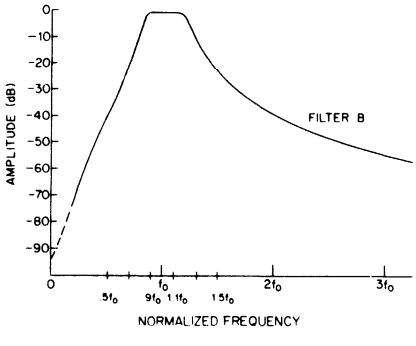
THE FOLLOWING SHOULD BE APPLIED IN TEST AND PRODUCTION CIRCUITS AS APPLICABLE.

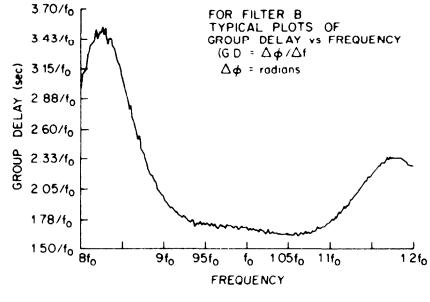
1) POWER SUPPLY RESISTORS MAY BE REQUIRED FOR TRANSIENT PROTECTION.

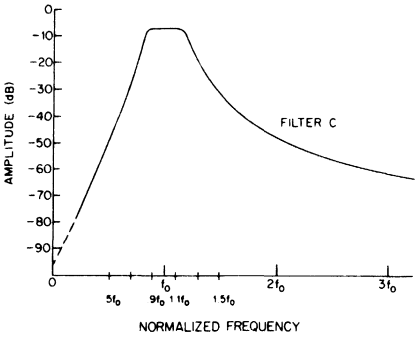
2) INPUT AND TRIGGER RESISTORS ARE REQUIRED IF SIGNALS MAY BE APPLIED WITH POWER OFF.

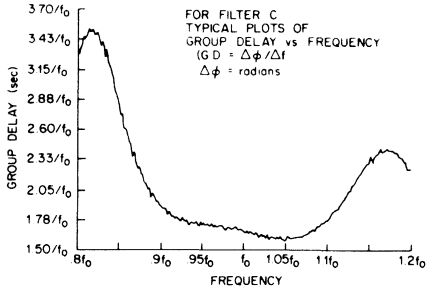




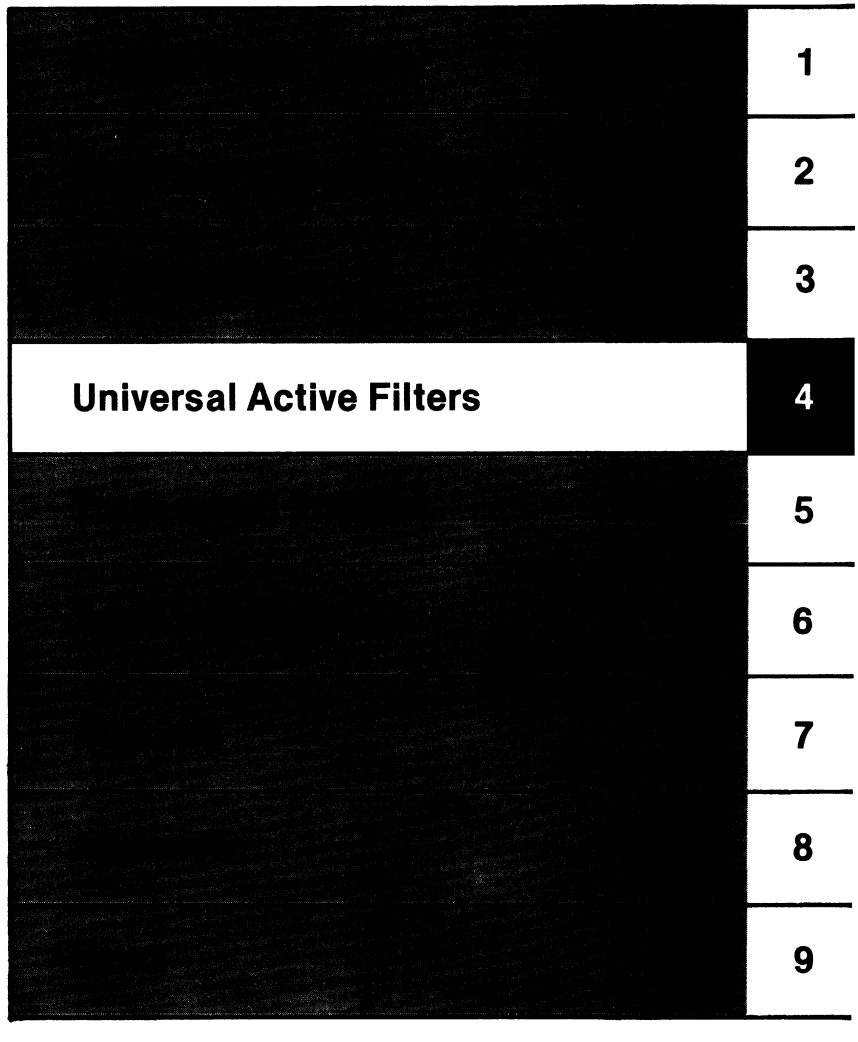








Analog Signal Processing Products



Description

The R5620 is a digitally programmable Universal Active Filter (UAF). It is implemented using Reticon's proven doubly-poly NMOS switched capacitor filter technology. It consists of a single second-order section with Q and f_0 programmable by separate 5-bit digital control words. Basic filter types are selected by hard wiring or switch selecting the filter inputs. Higher order filters can be obtained by cascading the R5620. Thus cascadability, microprocessor control, and universality make the R5620 an ideal, cost effective filter building block.

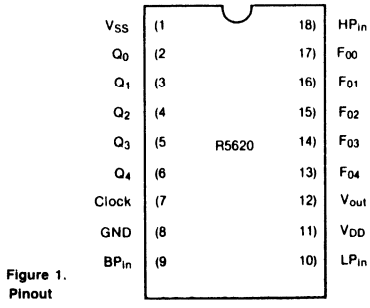


Figure 1. Pinout

Key Features

- Universal: Implement any classical filter
- Easy to use: No external components required
- Look up table responses: No calculations required
- Q and F_0 independently programmed
- Clock and control lines are TTL and CMOS compatible
- Small size: 18 pin DIP
- Low current consumption: Typically 4.5 mA
- Wide supply Voltage Range: ±5V to ±10V

Filter Types Available

- Low-pass
- Band-pass
- High-pass
- Low-pass elliptical *
- High-pass elliptical *
- Notch
- All-pass
- Programmable oscillator **

* These modes require external resistors
** This mode requires external gain

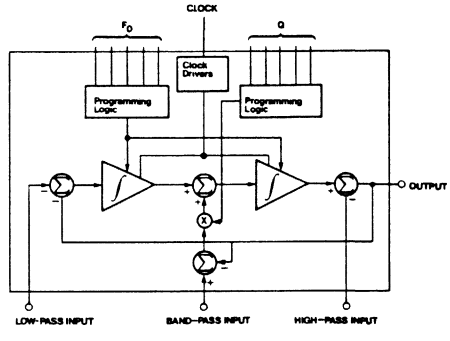


Figure 2. Functional Block Diagram

Device Operation

The Q and center frequency response of the filter are controlled by separate 5-bit digital inputs which may be microprocessor controlled or hard wired. The clock-to-center frequency ratio (f_C/f_0) can be varied from 50 to 200 in 32 logarithmic increments. The Q values are selectable in 32 approximately logarithmic increments, ranging from 0.57 to 85. The typical filter responses can be chosen from Table V, thus avoiding the cumbersome calculations and external components that other UAF devices require. The filter type is chosen by hard wire programming the filter inputs as shown in Table IV. For optimum performance, all unused inputs should be grounded.

Operational Considerations

Plots of typical amplitude, group delay, and phase responses are shown in Figures 6 through 10. THE PLOTS AND TRANSFER FUNCTIONS CONTAINED HEREIN ARE TYPICAL OF THOSE FOR A CONTINUOUS TIME ANALOG FILTER OF THE SAME ORDER, TYPE, AND Q. Some additional comments on filter response can facilitate design. Please note that items (a-d) are true for any second order analog filter:

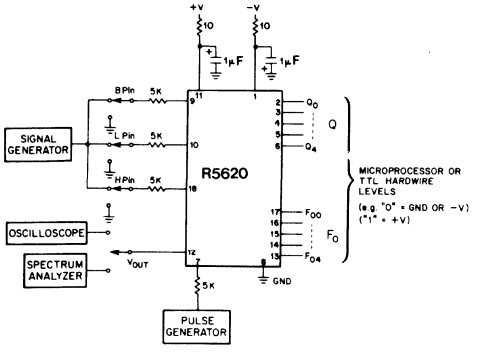
a. Band-pass and notch characteristics are most easily defined by the relation $Q = f_0/B.W.$ where B.W. = bandwidth measured across the −3 dB point.

b. Beyond the −3 dB points, the roll off rate is very Q and filter type dependent, i.e., Butterworth, Chebyshev, Cauer, etc. The type dependency on roll off rate is evident only if a filter is made by cascading sections.

For a single second order section and for low Q values (i.e., $Q < 1$), the "classical" asymptotic roll off rate is established as 6 dB/octave (20 dB/decade) for band-pass filters and 12 dB/octave (40 dB/decade) for non-elliptic low-pass and high-pass filters. For more exact information, refer to Figures 6 through 8.

c. Group delay is defined as the derivative of phase with respect to (angular) frequency, G.D. = $d\phi/d\omega$. Approximations can be derived from the phase plots (arc tangent of the transfer function) of Figure 9 and 10 in conjunction with the formula $(\Delta\phi/360°)/(2\pi\Delta f)$ = G.D. For a small incremental

4



Note: The following should be applied in test and production circuits as applicable.

1. Power supply resistors may be required for transient protection.
2. Input and trigger resistors are required if signals may be applied with power off, and there is not a resistor already in series with the input.

Figure 3. Test Circuit

change in frequency (Δf), this calculation is the slope of the curve on the phase plot at any given frequency. Plots of these calculations are shown in Figure 9. A practical alternative to this is to measure the envelope delay of a burst of oscillation. Often in signalling circuits, the relative group delay difference between two points in the passband is more important than the maximum absolute time delay through the filter.

d. Another time domain parameter is that of step response. The time required to settle or rise to 95% of a final output value is approximately $Q(1/f_0)$. Often this parameter is referred to as the filter settling time (not to be confused with op amp settling time). The most common application of this calculation occurs when either Q or f_0 programming is changed (i.e., a step input) and it is important to know how long before the output reflects the new programmed parameters. It is possible to foreshorten this by synchronizing a burst oscillation on the clock trigger input. In effect this speeds up the "clearing out" of the charge (flow) established by the previous programming.

e. Notch operation is not recommended for Q's > 20. A notch depth of −40 dB is typical and can be −50 dB to −60 dB for low values of Q.

f. By configuring the band-pass mode, a Q of 40, and feeding the output back to the input an oscillator is obtained. For stability reasons, oscillators above 10 KHz might require a gain stage between the output and input. The nominal gain is 1.1. This also applies to configurations with f_c/f_0 ratios.

Transfer Functions

The simplified R5620 transfer function contains the terms for any filter type:

$$H(s) = -\frac{s^2 - (\omega_0/Q)\,s + \omega_0^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2} = \frac{V_{out}}{V_{in}}$$

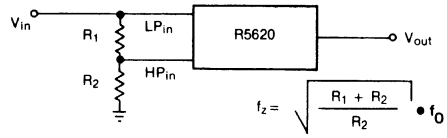


Figure 4. Low-Pass Elliptic Filter

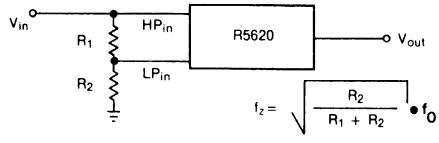


Figure 5. High-Pass Elliptic Filter

If a single filter type is desired, the other input pins are AC grounded, which is the same as multiplying the appropriate transfer function terms by zero. An all-pass filter is implemented if all three inputs are used. For the all-pass filter, the amplitude response is unity for all frequencies and the phase shift is adjustable by varying f_0 relative to a fixed frequency. To realize a notch filter, the band-pass input is grounded and the low-pass and high-pass inputs are tied together. The resistor implemented low-pass and high-pass elliptical responses are shown in Figure 4 and 5. The transfer function equations for the major filter types are shown below.

LOW-PASS

$$H(s) = \frac{\omega_0^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

LOW-PASS ELLIPTIC

$$H(s) = \frac{(\omega_0/\omega_z)\,s^2 + \omega_0^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

HIGH PASS

$$H(s) = \frac{s^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

HIGH-PASS ELLIPTIC

$$H(2) = \frac{s^2 + (\omega_z/\omega_0)\,\omega^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

BAND-PASS

$$H(s) = \frac{-(\omega_0/Q)\,s}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

ALL-PASS

$$H(s) = \frac{s^2 - (\omega_0/Q)\,s + \omega_0^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

NOTCH

$$H(s) = \frac{s^2 + \omega_0^2}{s^2 + (\omega_0/Q)\,s + \omega_0^2}$$

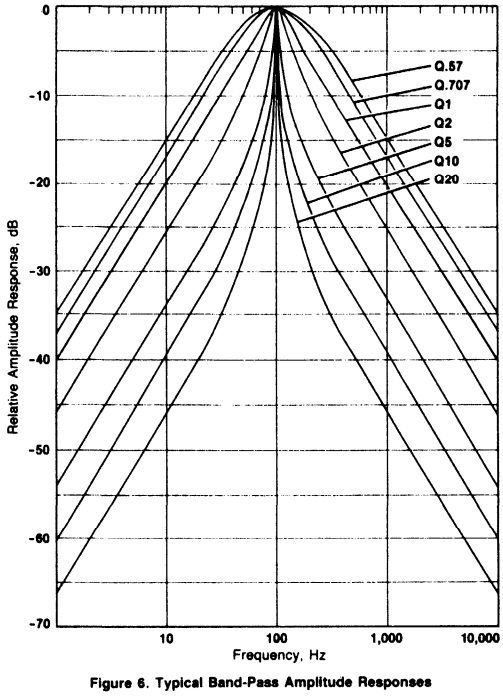


Figure 6. Typical Band-Pass Amplitude Responses

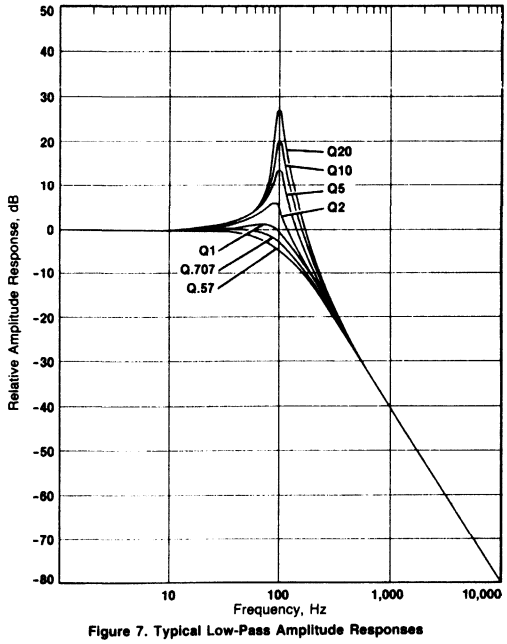


Figure 7. Typical Low-Pass Amplitude Responses

Practical Considerations

Tolerances - Design tolerances for f_C/f_0 and Q are typically ±1.5% and ±10% respectively. Device-to-device variations dominate these tolerances since, e.g., the typical temperature coefficient for f_C/f_0 is between 20-50 ppm/°C at $f_0 \leq 10$ KHz. The design values of f_C/f_0 may be more closely realized by utilizing the digital control words on the appropriate side of the design value. Another common method of adjusting the f_C/f_0 ratio is to vary the master clock by the desired amount. This later method is particularly helpful when evaluating the phase shift (measured at any given frequency in the pass band) due to device-to-device or temperature variations.

Aliasing and Reconstruction - If signals or noise exist near the sample rate or its harmonics, pre-filtering may be required to ensure that the difference (lower side band or beat) frequency(ies) don't fall or alias into the pass band. Since f_C/f_0 ratios of SCF's are relatively quite large, this can usually be accomplished with a simple RC filter. Typically, the corner frequency of the RC filter is chosen to be 2 to 10 times the corner frequency of the pass band.

In general, it is not necessary to provide antialias filtering between cascaded sections that have the same sample rates. Exceptions are cascaded high-pass sections, or low-pass sections when DC offset shifts are critical.

Post-filtering with an RC filter can minimize sample rate feed through (typically 30 mV.p-p) and can serve as a reconstruction or smoothing filter for the staircase sampled data output waveform. Using an RC corner frequency of less than 10 times greater than the pass band corner will improve antialiasing and reconstruction characteristics but will increase the risk of modifying pass band amplitude and phase performance.

Second-Order Effects - Departures from the programmed values of f_C/f_0 and Q are to be expected at low values of Q and f_C/f_0. Primarily these reflect the differences (mainly the need for compensation for the curved mapping of the $j\omega$ axis into the z-domain) between the s-domain used in state-variable filter analysis and the z-domain used to model the sampled data nature of SCF's. Typical effects of the interdependency of Q and f_C/f_0 are shown in Figure 12a, b. Table V already includes the necessary correction factors for Q as a function of f_C/f_0. Neither the table nor the figure include Q and f_C/f_0 error tolerances.

Active Element Limitations - Footnote 3 of Table II alludes to temperature dependent parameters of leakage current and transconductance. For example, leakage current roughly doubles for every 10°C rise in temperature. Thus to maintain a given leakage current level, the Clock Frequency and the corresponding f_C/f_0 should be changed by the same proportion. The maximum frequency limit for both parameters, for either high or low Q's should be lowered by approximately 20% when operating at 70°C.

For an insertion loss of less than 1 dB, the Load Impedance should be more than 1000 times the Load Impedance. When cascading sections, there is generally no problem since for

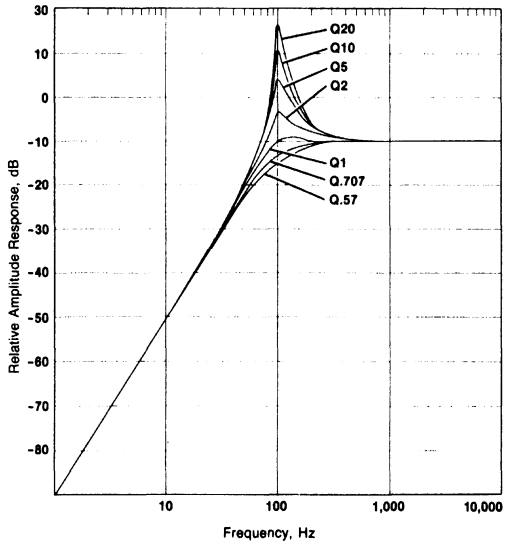


Figure 8. Typical High-Pass Amplitude Responses

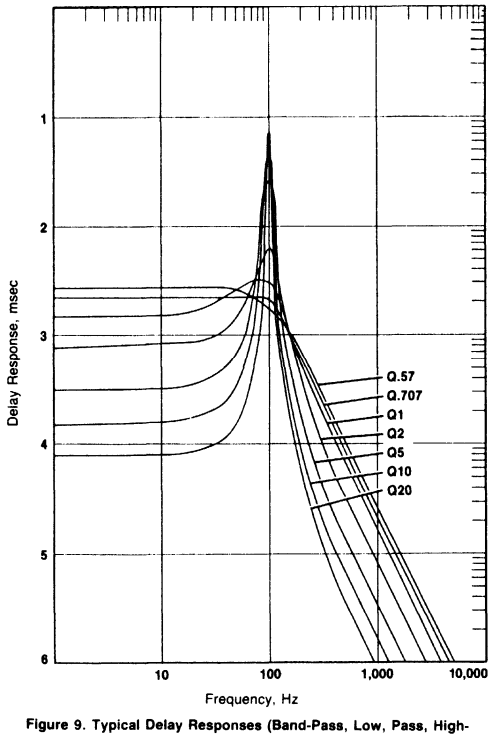


Figure 9. Typical Delay Responses (Band-Pass, Low, Pass, High-Pass)

almost all filter configurations and f_C/f_0 or Q programming, the Input Impedance is several megohms. Exceptions occur for some low-pass and band-pass modes where the impedance may fall to 480KΩ.

Sources of noise such as Harmonic Distortion, Clock Feed through, and Power Supply Ripple can generally be removed by various means. Noise that cannot be removed is that labeled Output Noise in Table III, which is broadband to 1/2 of the sample rate.

There are trade-offs between selecting a maximum f_C/f_0 and the gain of the internal op-amps at the upper frequency range.

To avoid detailed calculations, it is recommended to use an f_C/f_0 that is 75% of maximum.

Double poly NMOS capacitors are extremely stable over temperature. However, the impedances of parasitic capacitances (which affect Clock Feed through and Power Supply Ripple Rejection noise contributions) will vary in amplitude as a function of Clock Frequency or the frequency content of the Power Supply Ripple. Filtering of the power supply lines will minimize ripple noise and will help protect the device from random power line transients, including power up spikes.

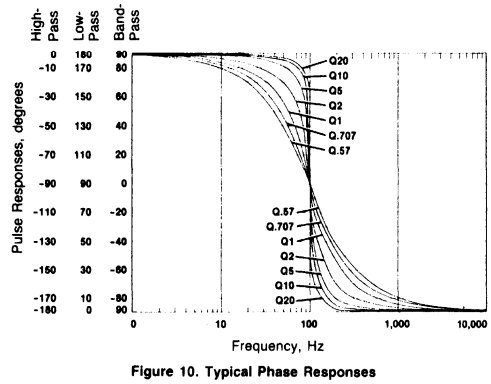


Figure 10. Typical Phase Responses

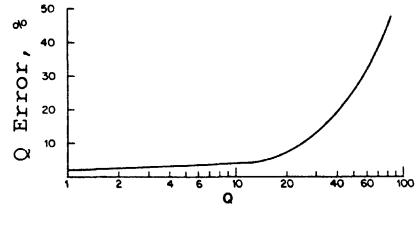


Figure 11. Typical Q Error as a Function of Q

TABLE I: ABSOLUTE MAXIMUM/MINIMUM RATINGS*

	Min	Max	Units
Input Voltage - any terminal with respect to substrate[1, 3]	−0.4	21	V
Output short circuit duration - any terminal	Indefinite		
Input/Output current - any terminal (externally forced)		10	mA
Power Dissipation [2]	500		mW
Storage Temperature	−55	125	°C
Operating Temperature	0	70	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C
CAUTION: Observe MOS Handling & Operating Procedures			

*Continued operation at these limits may cause permanent damage.

(1) Although devices are internally gate protected to minimize the possiblity of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS}V_{SS} + I_{ODD}V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

4

TABLE II: DEVICE CHARACTERISTICS & OPERATION RANGE LIMITS [1] R5620

Parameter	Conditions & Comments	Symbol	Min	Typ	Max	Units
Supply Voltages		$V_{DD}+$, $V_{SS}-$	±5		±10	V
Quiescent Current [2]	No load	I_Q		4.5		mA
Clock Frequency	$f_{clock} = 2 \times f_{sample}$ (f_S)	f_c	10 [3]		1250 [4]	KHz
Clock Pulse Width	Ext. drive	t_c	200		$10^9/f_c$-200	nS
Digital Input Threshold level (clock, Q, and F_C/f_0 control)		V_{TH}	0.8	1.6	2.0	V
Output Signal [3]	$R_L \geq$ 10K R_L = Zero Ω	V_o I_o		 4	14	V p-p mA
Center/Corner Frequency Range		f_0	1 [3]	See Table V	20,000 [4]	Hz
Q-Range			.57		100	
Input Impedance		R_i C_i		≥10	 ≤10	MΩ pF
Load Impedance(s)			>10		≤50	KΩ pF
Output Impedance	Small-signal	R_0		10-100		Ω
Output Offset Voltage(s)		V_{off}		50		mV

1. $V_{DD}+ = +10V$, $V_{SS}- = -10V$, $f_c/f_0 = 50$ Q = 1, $f_c = 50$ KHz, T = 25°C
2. Increase 15% for operation to 0°C
3. Performance degrades at temperatures above 25°C
4. For low value Q's, operation 2 MHz for f_c is possible

TABLE III: PERFORMANCE STANDARDS [1] R5620

Parameter	Conditions & Comments	Symbol	Min	Typ	Max	Units
Output Noise	B. W. = fs/2	e_n		0.27		mV_{rms}
Dynamic Range	V_0/e_n Q = 1 Q = 40	D.R.		94 84		dB dB
Total Harmonic Distortion	f_0 = 1 KHz	THD		−54		dB
Insertion Loss				0		dB
Clock Feedthrough				30	60	mV p-p

1. Measured with ±10V supplies, f_c/f_0 = 50; Q = .71; f_c = 50 KHz; T = 25°C.

TABLE IV FILTER SELECT TABLE

	Connections		
Filter Type	**LPin**	**HPin**	**BPin**
Lowpass	Vin	GND	GND
Highpass	GND	Vin	GND
Bandpass	GND	GND	Vin
Notch	Vin	Vin	GND
All-pass	Vin	Vin	Vin
Sine Wave * Oscillator	GND	GND	Vout

* Q must be set to 11101 for oscillator mode operation and external gain added to the feedback path.

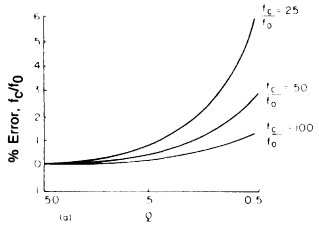


Figure 12a. Typical f_0 Error as a Function of Q

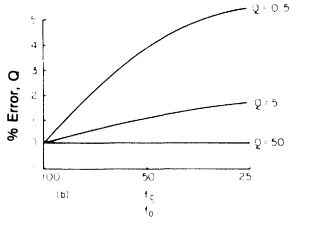


Figure 12b. Typical Q Error as a Function of f_c/f_0

TABLE V
R5620 Q, F_0 PROGRAMMING TABLE (TYPICAL VALUES)

Q (see figure 11)	Code $Q_4...Q_0$	F_c/F_0 (±1.5%)	Code $F_{04}...F_{00}$
.57	00000	200.0	00000
.65	00001	191.3	00001
.71	00010	182.9	00010
.79	00011	174.9	00011
.87	00100	167.2	00100
.95	00101	159.9	00101
1.05	00110	152.9	00110
1.2	00111	146.2	00111
1.35	01000	139.8	01000
1.65	01001	133.7	01001
1.95	01010	127.9	01010
2.2	01011	122.3	01011
2.5	01100	116.9	01100
3.0	01101	111.8	01101
3.5	01110	106.9	01110
4.25*	01111	102.3	01111
5.0	10000	97.8	10000
5.8	10001	93.5	10001
7.2	10010	89.4	10010
8.7	10011	85.5	10011
10.0	10100	81.8	10100
11.5	10101	78.2	10101
12.0	10110	74.8	10110
13.5	10111	71.5	10111
15.5	11000	68.4	11000
17.5	11001	65.4	11001
20.0	11010	62.5	11010
24.0	11011	59.8	11011
30.0	11100	57.2	11100
35.0	11101	54.8	11101
55.0	11110	52.3	11110
85.0	11111	50.0	11111

EG&G RETICON R5621/5622 RESISTOR PROGRAMMABLE UNIVERSAL ACTIVE FILTERS

KEY FEATURES

- **Easy to use.**
- **Small size: 14 or 20 pin DIP.**
- **Low power consumption: as low as 25 mw per package.**
- **Wide power supply range: ±5 to ±10.**
- **Up to four 2-pole sections per package.**
- **High dynamic range: up to 96 dB.**
- **Wide signal range: 0.1 Hz to 30 KHz.**
- **Low cost.**
- **Low sensitivity to external component variation.**
- **Wide Q range: 0.5 up to 500.**
- **Wide clock to center/corner frequency range: 25:1 to over 100:1.**
- **Clock to center frequency accuracy ≤0.5% (device to device).**

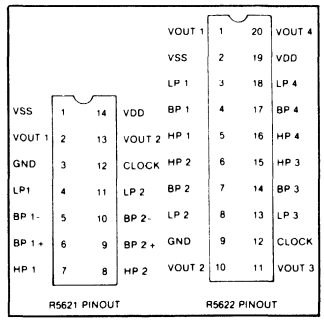


Figure 1. Pinout Diagrams

FILTER TYPES AVAILABLE

	R5621	R5622
Lowpass	yes	yes
Bandpass	yes	yes
Highpass	yes	yes
Lowpass elliptical	yes	yes
Highpass elliptical	yes	yes
Notch	yes	yes
Oscillator	yes	no
Allpass	yes	no
Biquad	yes	no

DESCRIPTION

The R5621 and R5622 are double-poly NMOS resistor programmable switched capacitor universal active filters. The R5621 consists of two second order state variable filters packaged in a 14 pin DIP. The R5622 is a quad second order section (four 2-pole filters) housed in a 20-pin DIP. With only an external clock and up to seven external resistors, any classical filter type can be configured. Center frequencies of all filter types including allpass and notch can be adjusted by changing the external resistor ratios or varying the clock frequency. Therefore, filter accuracy and stability are relatively insensitive to component variations. Filter Q's are also adjustable using resistor ratios. The filter sections are cascadable and up to an eighth order filter may be achieved with only one package.

4

DEVICE OPERATION

The R5621 and R5622 resistor programmable universal active filters are based on a two integrator state variable second order switched capacitor filter. (See Figure 2.) The time constant is controlled by the sample rate applied to the filters and is nominally a clock to corner ratio of 25 to 1. All of the standard filter transfer function characteristics can be controlled by feeding back the output signal to the four inputs. For example, the gain from Vout to LP controls the filter clock to center ratio. If Vout is applied directly to LP, then the clock to center frequency ratio is 25 to 1. If a resistor divider is tied between Vout and LP then the clock to center frequency ratio can be adjusted to a value greater than 25 to 1. If the input signal is also resistor summed into this junction then a lowpass filter is implemented.

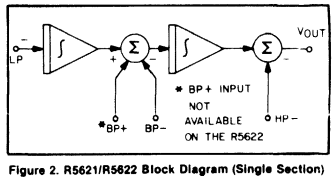


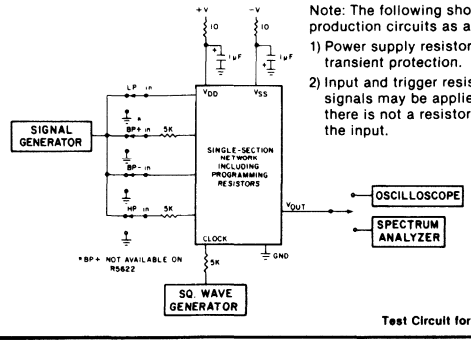
Figure 2. R5621/R5622 Block Diagram (Single Section)

The gain from Vout to BP- can be used to control the Q of the second order section. If Vout is tied directly to BP- then the Q is nominally 0.5 (this will vary as a function of feedback to LP). If a resistor divider is tied between Vout and BP- then the Q can be adjusted to a value greater than 0.5. If the input signal is resistor summed into this input, then an inverting bandpass filter can be implemented. The BP+ and HP inputs are used primarily as inputs for the highpass and non-inverting bandpass modes, however, the BP+ input can be fed signals from Vout to implement a sine wave oscillator.

OPERATIONAL CONSIDERATIONS

The optimal clock to center frequency ratio of the R5621 and R5622 is 50 to 1. This ratio will yield maximum p-p output signal and dynamic range. Dynamic range will drop about 6 dB for each halving or doubling of this ratio.

Selection of resistor values is also important. The total parallel resistance on the output should be kept above 10KΩ so that the maximum output signal swing will not be reduced. The parallel combination of all resistors going to a summing junction (BP- or LP) should be less than 100 KΩ to reduce input noise. In all cases, unused inputs should be grounded to



Note: The following should be applied in test and production circuits as applicable.

1) Power supply resistors may be required for transient protection.

2) Input and trigger resistors are required if signals may be applied with power off, and there is not a resistor already in series with the input.

Test Circuit for R5621/R5622 (Single Section)

TABLE I: ABSOLUTE MAXIMUM/MINIMUM RATINGS

	Min	Max	Units
Input Voltage—any terminal with respect to substrate(1)(3)	-.4	21	V
Output short circuit duration—any terminal		Indefinite	
Input/Output current—any terminal (externally forced)		10	mA
Power Dissipation(2)	500		mW
Storage Temperature—plastic —ceramic	-55	125	°C
Operating Temperature—plastic	0	70 125 °C	°C
Junction Temperature (chip)		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C

CAUTION: Observe MOS Handling & Operating Procedures

(1) Although devices are internally gate-protected to minimize the possibility of static damage, MOS handling precations should be observed.

(2) This rating is pertinent only when external circuitry force the device to absorb power. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., I_{QSS} V_{SS} + I_{QDD} V_{DD}) plus a percentage of output load power which reflects the efficiency of the output driver. Under worse case loads or temperature the package limitations prevail.

(3) Do not insert or remove device from socket while under power.

TABLE II: DEVICE CHARACTERISTICS & OPERATION RANGE LIMITS (1) R5621/R5622

PARAMETER	CONDITIONS & COMMENTS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltages		V_{DD} + V_{SS} -	5 -5		10 -10	V V
Input Bias Current		I_{SB}		0.1		μA
Quiescent Current(2) R5621	No load ±5V ±10V	I_Q		2.5 4.0		mA mA
R5622	±5V ±10V			4 6.6		mA mA
Clock Frequency	f_{clock} = f_{sample}	f_c	0.025 (3)		750. (4)	KHz
Clock Pulse Width	Ext. drive	tc	50% duty cycle square wave			
Input Clock Threshold level		V_{TH}	0.8	1.6	2.0	V
Output Signal (3)	$R_L \geq 10K\Omega$ R_L = Zero Ω	V_O I_O		5	14	V p-p mA
Center/Corner Frequency Range		f_0	1.0 (3)		30,000(4)	Hz
Q-Range			0.5		500	
Input Impedance(s)		R_i		1		MΩ
Load Impedance(s)			>10			KΩ
Output Impedance	Small-signal	R_0		10		Ω
Output Offset(5) Voltage(s)	R5621 R5622	V_{off}		100 20		mV mV

(1) V_{DD} + = 10V, V_{SS} - = -10V, f_c/f_0 = 50 Q = 1, f_c = 50 KHz, 25 °C

(2) Increase 15% for operation to 0 °C

(3) Performance degrades at temperatures above 25 °C. Lower frequency operation available on special order.

(4) for low Q values only (≤2). High Q values for center frequencies below 20 KHz and sample rates below 500 KHz.

(5) For $f_c/f_0 \leq 100:1$

TABLE III: PERFORMANCE STANDARDS (1) R5621/R5622

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
Output Noise (1)			0.240		mV_{rms}
Power Supply Ripple Rejection (1) V_{SS}		10			dB
V_{DD}		30			dB
Dynamic Range (1)	D.R.		96		dB
Total Harmonic Distortion (1) @ f_0 = 1KHz	THD			-58	dB
Crosstalk				-75	dB
Clock Feedthrough			30		mV p-p

(1) Measured with ±10 volt supplies, Q = 1, f_c/f_0 = 50, fc = 50 KHz. Performance will degrade with higher Q's and lower or higher fc/fo. Dynamic range is P-P signal to RMS noise to 1/2 of the sample rate.

prevent crosstalk from these pins. (See Table IV).

When high accuracy filters are being designed, the special characteristics of switched-capacitor filters should be considered. The equations describing the clock to center frequency ratio are accurate for filters that have high Q's (>5) and large clock to center frequency ratio's (fc/f0 >50 to 1). Filters that do not fall into these two catagories may have significant errors due to the sampled data effects that are characteristic of all switched capacitor filters. (See Figure 3). Once the final filter design is established, center frequency tolerance for the filter chips (not including external resistor tolerances) will be less than ±0.5%.

ALIASING CONSIDERATIONS

As with all sampled data devices, care should be taken to prevent aliasing of signals into the passband. If signals exist near the sample rate or its harmonics that might be aliased into the passband, then prefiltering is required. Since clock to center frequency ratios on switched-capacitor filters are quite large, this can usually be accomplished with a simple RC filter. The output of the devices will contain sample rate feedthrough at about 30 mv P-P. If this noise can affect system performance, it should be removed. Once again, a simple RC is usually adequate. When cascading second order sections that have the same sample rate, it is only necessary to provide anti-alias filtering to the first filter section.

TRANSFER FUNCTIONS

LOWPASS:

$$H(s) = -\frac{\omega_0^2}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

BANDPASS:

$$H(s) = -\frac{-(\omega_0/Q)\,S}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

HIGHPASS:

$$H(s) = -\frac{S^2}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

LOWPASS ELLIPTIC:

$$H(s) = -\frac{(\omega_0/\omega_z)^2\,S^2 + \omega_0^2}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

HIGHPASS ELLIPTIC:

$$H(s) = -\frac{S^2 + (\omega_z/\omega_0)^2\,\omega_0^2}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

NOTCH:

$$H(s) = -\frac{S^2 + \omega_0^2}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

ALLPASS:

$$H(s) = -\frac{S^2 - (\omega_0/Q))S + \omega_0^2}{S^2 + (\omega_0/Q)\,S + \omega_0^2}$$

DESIGN PROCEDURE

All of the resistor values that determine filter parameters such as clock-to-center or corner frequency ratio (f_c/f_0), Q and elliptic notch frequency (fz) can be calculated from simple equations.

The most general equations are listed under the biquad filter type and should be used if the simplified equations are not suitable. Any filter type utilizing the BP+ input is not available with the R5622. Detailed programming instructions for each filter type is described below.

I. General Design Procedure

A. Select f_0, f_c, Q, and fz (if required).

B. Calculate the "K_1" values using the desired f_0, f_c.

C. Calculate the "K_2" values using the desired Q, plus K_1.

D. Select values for R_1 and R_4 in accordance with the resistor limits in Table IV.
Note: (1) For Elliptic Lowpass filters, calculate the "K_3" values using the desired fz, f_0.
(2) For Elliptic Highpass filters, calculate values for R_1 and R_2 before calculating the values of R_3 and R_6.

E. Calculate R_3 and R_6 using the "K" values determined in Steps B and C.

TABLE IV RESISTOR LIMITS

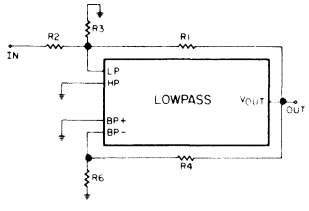
Resistor	Min	Max
R_1	20K	100K
R_2	*	∞
R_3	0	∞
R_4	20K	100K
R_5	*	∞
R_6	0	∞
R_7	*	100K
R_8	0	∞
R_9	*	100K
R_{10}	0	∞

* Value depends on driving capability of external circuitry. If preceding stage is an R5621 or R5622, then the minimum is 20KΩ.

NOTE: All programming schematics are for single section only. Repeat as required.

NOTE: $\frac{f_c}{f_0} \geq 36$

For lowpass, lowpass elliptical, highpass elliptical, allpass and notch filters. This limitation due to the particular ratio of R_1 and R_2 and allows realizable values of R_3. Other minimum values of $\frac{f_c}{f_0}$ can be obtained by using other values of R_1 and R_2 in the basic biquad equations.

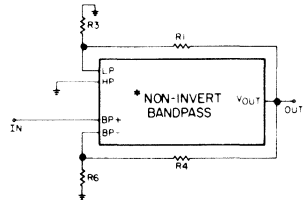


Assumption(1) $R_1 = R_2$; DC Gain = Unity

$$f_0 = \sqrt{K_1''} \cdot \frac{f_c}{25} \qquad K_1'' = \frac{R_3}{R_1 + 2R_3}$$

$$Q = \frac{\sqrt{K_1''}}{K_2'} \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

(1) If a gain other than unity is desired then gain = $\frac{R_1}{R_2}$ and K_1 from the biquad equations should be substituted for K_1''



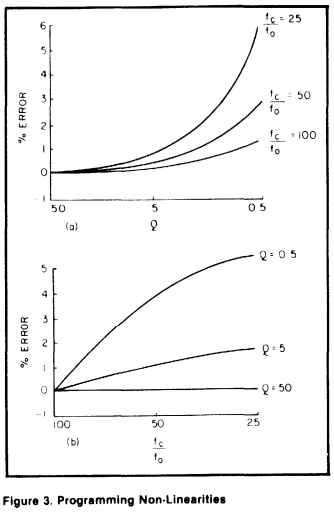
Gain (1) = $\frac{1}{K_2'}$ $\qquad K_1' = \frac{R_3}{R_1 + R_3}$

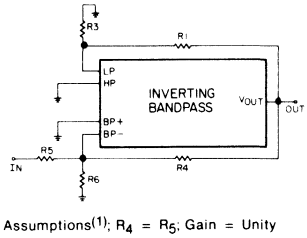
$$f_0 = \sqrt{K_1'} \cdot \frac{f_c}{25} \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

$$Q = \frac{\sqrt{K_1'}}{K_2'}$$

(1) Gain may be adjusted independent of Q using the resistor divider described by K_5 from the biquad equations.

*Not available on the R5622



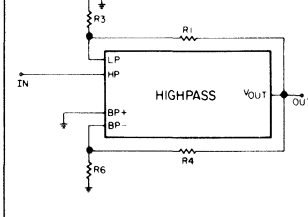


Assumptions(1); $R_4 = R_5$; Gain = Unity

$$f_0 = \sqrt{K_1'} \cdot \frac{f_c}{25} \qquad K_1' = \frac{R_3}{R_1 + R_3}$$

$$Q = \frac{\sqrt{K_1'}}{K_2''} \qquad K_2'' = \frac{R_6}{R_4 + 2R_6}$$

(1) For gains not equal to unity, gain = R_4/R_5 and K_2'' should be replaced with K_2 from the biquad equations.

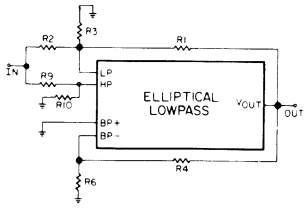


Gain = Unity

$$f_0 = \sqrt{K_1'} \cdot \frac{f_c}{25} \qquad K_1' = \frac{R_3}{R_1 + R_3}$$

$$Q = \frac{\sqrt{K_1'}}{K_2'} \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

Figure 3. Programming Non-Linearities



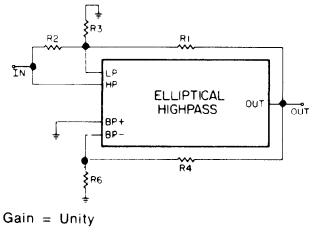
DC Gain [1] = Unity; $R_1 = R_2$

$$f_0 = \sqrt{K_1''} \bullet \frac{fc}{25} \qquad K_1'' = \frac{R_3}{R_1 + 2R_3}$$

$$Q = \frac{\sqrt{K_1''}}{K_2'} \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

$$f_z = \sqrt{\frac{1}{K_3}} \bullet f_0 \qquad K_3 = \frac{R_{10}}{R_9 + R_{10}}$$

(1) For gain other than unity, gain = R_1/R_2 and K_1 should be substituted for K_1''. The $\sqrt{1/K_3}$ term should also be multiplied times the gain.



Gain = Unity

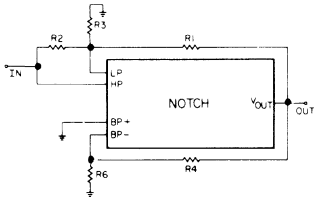
(1)

$$f_0 = \sqrt{K_1} \bullet \frac{fc}{25}$$

$$Q = \frac{\sqrt{K_1}}{K_2'} \qquad K_1 = \frac{R_2\ R_3}{R_1\ R_2 + R_1\ R_3 + R_2\ R_3}$$

$$f_z = \sqrt{\frac{R_1}{R_2}} \bullet f_0 \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

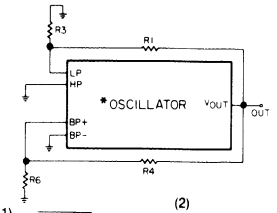
(1) For this case only, the resistor value R_1 and R_2 should be determined for f_z before the resistor values for f_0 (R_3) are calculated.



Gain = Unity; $R_1 = R_2$

$$f_0 = \sqrt{K_1''} \bullet \frac{fc}{25} \qquad K_1'' = \frac{R_3}{R_1 + 2R_3}$$

$$Q = \frac{\sqrt{K_1''}}{K_2'} \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

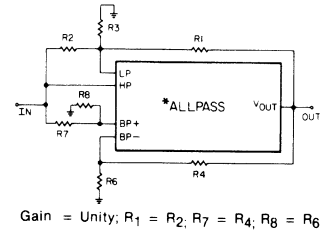


(1) $f_0 \cong \sqrt{\frac{R_3}{R_1 + R_3}} \bullet \frac{fc}{25}$ (2) $\frac{R_4}{R_6} \cong 20$

*Not available on R5622

(1) f_0 is also a function of the feedback coefficient defined by R_4 and R_6 and can vary considerably from the calculated value. For a fixed feedback coefficient, f_0 will not vary by more than ± 1%.

(2) The distortion of the sine wave can be adjusted by varying this ratio.

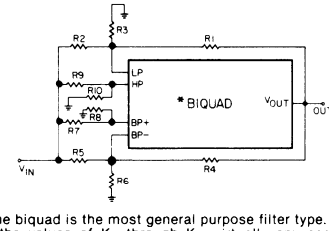


Gain = Unity; $R_1 = R_2$; $R_7 = R_4$; $R_8 = R_6$

$$f_0 = \sqrt{K_1''} \bullet \frac{fc}{25} \qquad K_1'' = \frac{R_3}{R_1 + 2R_3}$$

$$Q = \frac{\sqrt{K_1''}}{K_2'} \qquad K_2' = \frac{R_6}{R_4 + R_6}$$

*Not available on the R5622



The biquad is the most general purpose filter type. By adjusting the values of K_1 through K_6, virtually any second order transfer function can be achieved. In some cases it may be necessary to use an inverting op amp to achieve the correct polarity on these constants.

*The term defined by K_5 is not available on the R5622.

$$VOUT = VIN \left[\frac{- K_3 S^2 - K_4 S \frac{fc}{4} + K_5 S \frac{fc}{4} - K_6 \frac{fc^2}{16}}{S^2 + K_2 S \frac{fc}{4} + K_1 \frac{fc^2}{16}} \right]$$

$$K_1 = \frac{R_2\ R_3}{R_1\ R_2 + R_1\ R_3 + R_2\ R_3} \qquad K_4 = \frac{R_4\ R_6}{R_4\ R_5 + R_4\ R_6 + R_5\ R_6}$$

$$K_2 = \frac{R_5\ R_6}{R_4\ R_5 + R_4\ R_6 + R_5\ R_6} \qquad K_5 = \frac{R_8}{R_7 + R_8}$$

$$K_3 = \frac{R_{10}}{R_9 + R_{10}} \qquad K_6 = \frac{R_1\ R_3}{R_1\ R_2 + R_1\ R_3 + R_2\ R_3}$$

ADVANCE DATA

DESCRIPTION

The R5626 is the analog counterpart to digital gate array. It is a semi-custom switched-capacitor filter (SCF) array with on-chip capability for both analog and logic functions. All functions can be customized by a single mask, which will be used to complete inventoried pre-processed wafers. Advanced automated design programs are used to generate the metal mask given *user* supplied filter coefficients and logic equations or schematics. This means low cost and fast turn around for innumerable signal processing circuits.

The R5626 consists of:

a) 14 second-order SCF sections

b) Minimum of 3 uncommitted op-amps (more from unused sections)

c) 20 digital state cells with 6 I/O buffers

d) Sampling clock options

- TTL/CMOS master clock with ÷ 256 chain
- Crystal oscillator with ÷ 256 chain

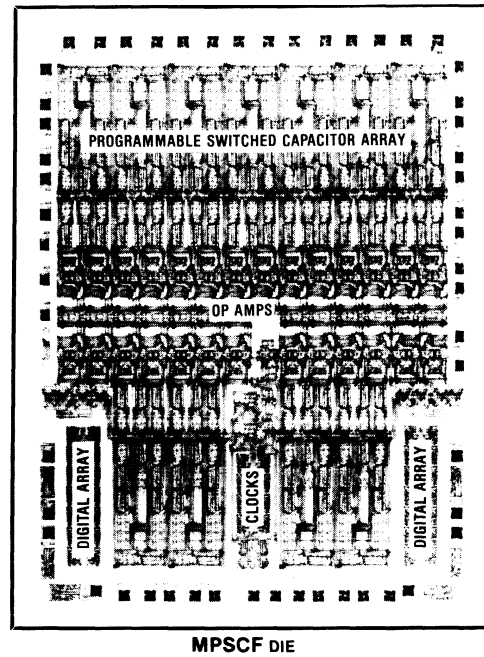
With the above features, the customized circuitry can:

1) be cascaded to implement higher order filters, including any classical filter type.

2) realize composite filters, minimizing circuit real estate.

3) allow for non-filtering circuit functions such as modulation, gain control, signal steering, gating, and multiplexing, etc.

Packaging for the R5626 is in a 24-pin DIP or larger (40 pads are available). Delivery is 6-8 weeks after completion of mask design.



MPSCF DIE

TYPICAL APPLICATIONS

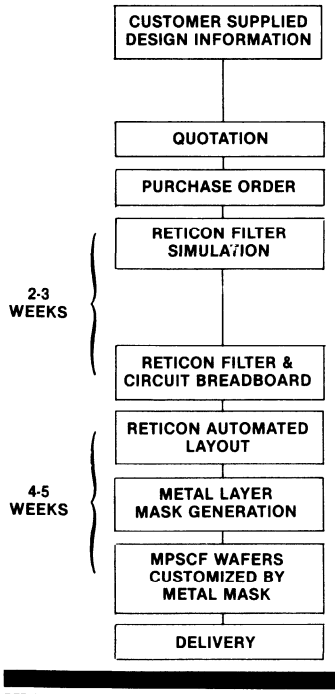
- **State-Variable Filters - All types, integrators, differentiators, inductance simulator, capacitance multipliers**
- **Tracking filters**
- **Baseband modulators**
- **Demodulators and detectors, zero crossing, peak detectors, and FSK schemes**
- **C-message and 1010 notch filter**
- **Programmable active filters**
- **Equalizers**
- **Spectrum analyzer (single chip)**
- **Hilbert Transformer**
- **Dynamic peak detection, limiters, and comparators**
- **Multiplexors, transmission gate switches, and S/H amps**
- **DTMF filters**
- **Ladder filters**

R5626 MASK PROGRAMMABLE SWITCHED CAPACITOR FILTER ARRAY

KEY FEATURES

- **Double Poly NMOS fabrication**
- **Automated metal mask: fast turnaround**
- **High dynamic range: Up to 85 dB**
- **Low Power: As low as 0.25 mA/pole**
- **No external components required**
- **Wide power supply range: ±5V to ±10V DC**
- **Low total harmonic distortion**
- **Wide center/corner frequency range: 0.05 Hz to 30 KHz**
- **Low cap ratio temperature sensitivity**
- **Wide Q range: 0.1 to 250**
- **Wide clock to center/corner frequency range: 15:1 to over 100:1**
- **Center frequency accuracy ±1%**
- **Q accuracy: typically ±1%**
- **Low 1/f noise**

R5626 MPSCF DEVELOPMENT CYCLE



Center/corner frequency, (f_0), Q, Voltage Levels (Gain), S/N, number of 2nd order sections, necessary interconnections and signal frequency range(s), schematic or Logic diagram for non-filter circuits. This information should take into account a tolerance of ±1% for f_0 and ±.1% to ±2% for Q's from .1 to 250.

f_0 and Q parameter transformation from the *s* domain to the *z* domain. Optimize capacitor ratios for accuracy and minimum parasitic coupling. Determination of proper ordering and stage gain(s) for a maximum S/N. The final output of this section are phase and attenuation versus frequency plots.

Confirmation of both filter and non-filter circuit performance.

CAD Digitizing/layout generation

Mask checking

Final layer processing

055-0129
38353

Analog Signal Processing Products

Key Features

- Provides the real and imaginary convolutions necessary for the chirp Z transform algorithm.
- Two 512-stage charge-coupled devices.
- Four mask-programmed transversal filters.
- Balanced differential outputs.
- Dynamic range (peak signal to rms noise) of 60 dB.
- Sampling rates 4 KHz to 2 MHz.
- Filter weighting coefficient accuracy of eight bits plus sign.
- 22-pin dual-in-line package.

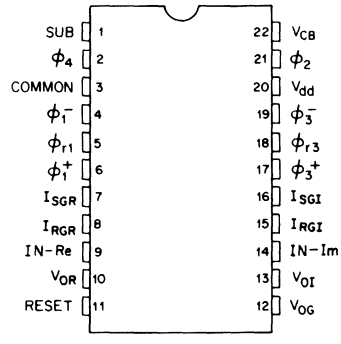


Figure 1. Pin Designations for R5601A.

Introduction

The R5601A is an MOS integrated circuit which can be used to perform the bulk of the computation required in the calculation of a 512-point Discrete Fourier Transform (DFT).[1] This circuit contains two separate 512-stage charge-coupled devices which are used to implement four transversal filters using the split-electrode weighting technique.[2] The filter weighting coefficients and internal circuit connections are configured so that this device, with additional off-chip components, can implement the chirp Z transform (CZT) algorithm to calculate a 512 point DFT.[2]

There are two versions of the R5601A which are available. They differ in the type of window which is effectively applied to the data to be transformed. The R5601A-1 uses a rectangular window for maximum resolution in the transform (or frequency) domain with the disadvantage of relatively high sidelobe response (frequency leaks).[3] The R5601A-2 uses a Hanning window in order to decrease these sidelobes. However, this window also decreases the frequency resolution of the resulting DFT by about a factor of two. In general, the R5601A-2 is intended for use in spectral analysis applications and the R5601A-1 for direct calculation of the complex Fourier coefficients. The R5601A-2 is arranged to minimize the high-frequency losses in the filters, with the result that low frequency components correlate at mid scan instead of at scan ends. The frequency scales are thus arranged in different order for the two versions. The weighting coefficient equations show the distinction.

The use of analog discrete time techniques to calculate Fourier spectra allows an enormous reduction in hardware complexity and, therefore, cost when compared to all-digital techniques. This approach should find application whenever low cost, reduced size, high speed, or low power requirements are important.

Device Description

The R5601A is available in a 22-pin DIP package with connections as shown in Figure 1. The functions of the pins are given in Table I and a simplified block diagram in Figure 2. NOTE: All real and imaginary pin designations are interchanged from those of the older R5601. This change merely corrects the designations; it does not change the construction or interchangeability of the old and new devices. The timing diagram is shown in Figure 3 and a typical connection arrangement in Figure 4. Figures 5 and 6 depict the device geometry and the I/O circuits. The chip contains two CCD channels lying adjacent to each other. Figure 5 is an edge view of the chip which has been cut along the length of the channels to exhibit the four-phase clock gates which are driven by an external clock to transfer the signal charge. The input signal gates, I_{SGR} and I_{SGI}, for real and imaginary channels, respectively, are clocked with the same phase as $\varnothing_2$; therefore, the signal is sampled into both channels when $\varnothing_2$ goes low. These discrete signal packets then pass under the input receiving gates, I_{RGR} and I_{RGI}, which are the receiving gates for the real and imaginary channels respectively, then sequentially transfer down the channel through the potential wells which are formed under each of the four clock phases, $\varnothing_1$, $\varnothing_2$, $\varnothing_3$, and $\varnothing_4$, through clocks applied from an external source. After transferring through the channel, the signal terminates into V_{DD} through the output gate, V_{OG} and the switch labeled RESET. The delay line outputs, labled V_{OI} and V_{OR}, are required only during testing and initial adjustment.

Figure 6 depicts the top view of a single CCD channel and demonstrates the split-electrode technique which implements the two different filters on each channel. The weighting coefficients of these filters are determined by each major clock-gate electrode which is split with weighting proportional to the difference in the lengths. The chirp waveform in dotted lines emphasizes the two separate weighting functions on the same channel, one weighting effective during $\varnothing_1$'s high state, and the other effective during $\varnothing_3$'s high state.

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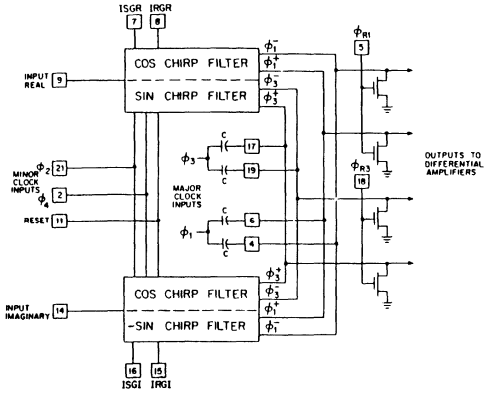


Figure 2. Simplified Block Diagram of R5601A.

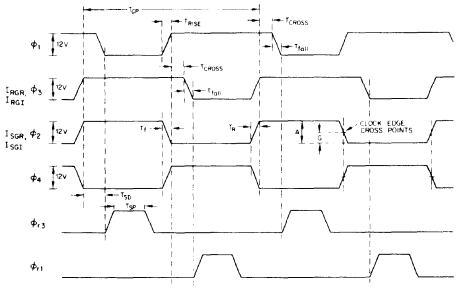


Figure 3. Clock Waveforms and Timing Diagram

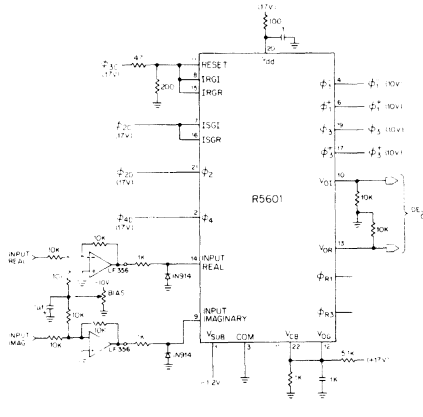
1. $\varnothing_1$ & $\varnothing_3$ Clock Transition (a_1) 50 $\leq T_{CROSS} \leq T_{CP}/8$
   (b_1) $10 \leq T_{RISE} \geq 50$ (c_1) $50 \leq T_{fall} \leq 100$
2. $\varnothing_2$ & $\varnothing_4$ Clock Transition (a_2) $10 \leq T_f \leq 50$
   (b_2) $10 \leq T_R \leq 50$ (c_2) $0.3A \leq G \leq 0.6A$
3. $\varnothing_{r1}$ & $\varnothing_{r3}$ Clock Transition (a_3) $30 \leq T_{SD} \leq T_{CP}/8$
   (b_3) $100 \leq T_{SP} \leq T_{CP}/2$

NOTE: All time dimension in nanosec.

In order to perform the Fourier transform, it is necessary to multiply the input signal by a complex chirp waveform, convolve the real and imaginary parts with a second complex chirp waveform and then post multiply the output by the same chirp waveform used in the pre-multiplication. The R5601 performs the convolution of the real and imaginary input signals with a complex chirp $[e(i\pi n^2)/N,\ 1 \leq n \leq 512$ for the R5601A-1]. If only the magnitude of the spectrum is required, then the filter outputs are squared and summed. This is true for both the R5601A-1 and R5601A-2. Block diagrams for calculating the power spectra $|F_k|^2$ and the complex Fourier coefficients F_k are shown in Figure 7. The major computational task—the complex convolution—is performed by the R5601A convolution filter shown with the dash-line rectangle.

To perform the convolution, the R5601A device contains four 512-stage CCD mask-programmed transversal filters which are implemented using two CCD delay lines. The two different filter functions on each CCD are programmed by splitting the $\varnothing_1$ and $\varnothing_3$ clock electrodes which are labeled ($\varnothing_1+$, $\varnothing_1-$ and $\varnothing_3+$, $\varnothing_3-$) as shown in Figure 6. The effective multiplying factor, called the weighting coefficient, is proportional to the difference in size of the two portions of a particular electrode. These weighting coefficients are programmed to an accuracy of eight bits plus sign (i.e., 512 possible levels). Since the value of the weights are determined by the pattern of one mask used in the semiconductor fabrication process, it is expected that this accuracy level will be independent of minor fabrication variations and will be easily reproducible.

The sampled analog signal moves down the analog delay line under control of the four clock phases, $\varnothing_1$, $\varnothing_2$, $\varnothing_3$, and $\varnothing_4$ (see Figure 5). The $\varnothing_1$ clock drive should be capacitively coupled by two capacitors to the programmed split electrodes $\varnothing_1+$ (Pin 6), and $\varnothing_1-$ (Pin 4) which are also the output signal lines. This is also true for the $\varnothing_3$ clock and the split electrodes $\varnothing_3+$ and $\varnothing_3-$. The values of the external capacitors are 500 pf. Pins 8, 11, and 15 also require the $\varnothing_3$ clock waveform, but it should come from a different driver device than the one used for $\varnothing_3+$ to insure isolation of the output from the input.



NOTES:
1. COMPONENT VALUES ARE TYPICAL.
2. "2" IS SAME WAVEFORM BUT SEPARATE DRIVER. E.G. ϕ_{3c} SAME WAVEFORM AS ϕ_3.
3. IRGR = INPUT RECV. GATE/REAL
   IRGI = INPUT RECV. GATE/IMAG.
   ISGR = INPUT SAMPLE GATE/REAL
   ISGI = INPUT SAMPLE GATE/IMAG.
4. ( ) INDICATES TYPICAL VOLTAGE LEVEL

Figure 4. Connection Arrangement for R5601A.

The outputs from the split electrodes, i.e., $\varnothing_1+$ and $\varnothing_1-$, $\varnothing_3+$ and $\varnothing_3-$, are appropriately summed together on the chip. The output from similar clock electrodes, for example $\varnothing_1+$, of the two different delay lines are brought to the same point on the chip (see Figure 6). This connection performs the summing of the signals. In the typical configuration, the ouput from $\varnothing_1+$ and $\varnothing_1-$ are differentially combined and then sampled and held until $\varnothing_3$ data is valid. The $\varnothing_3+$ and $\varnothing_3-$ are also differentially combined to produce the other output signal. Two more clock signals, $\varnothing_2$ and $\varnothing_4$, are minor phases required to drive these devices (see Figure 5). Two off-chip differential amplifiers with a gain of approximately 10 for R5601A-1 or 20 for the R5601A-2 are required to obtain the output signals of five volts maximum amplitude.

The analog input signals into the CCD device are superimposed on an approximately 9-volt dc bias level and can swing more than three volts peak-to-peak. The input circuitry is designed to be compatible with the split-

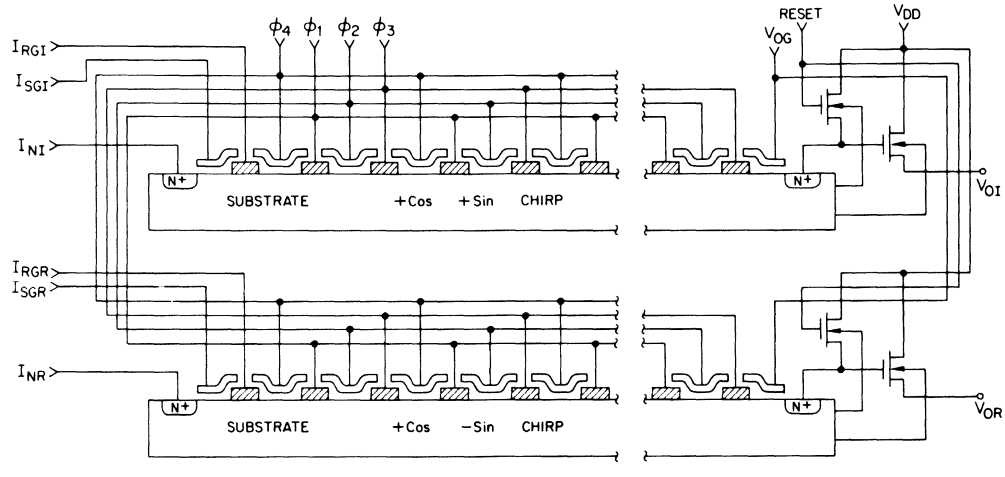


Figure 5. Schematic Layout of the CCD Channels, edge view.

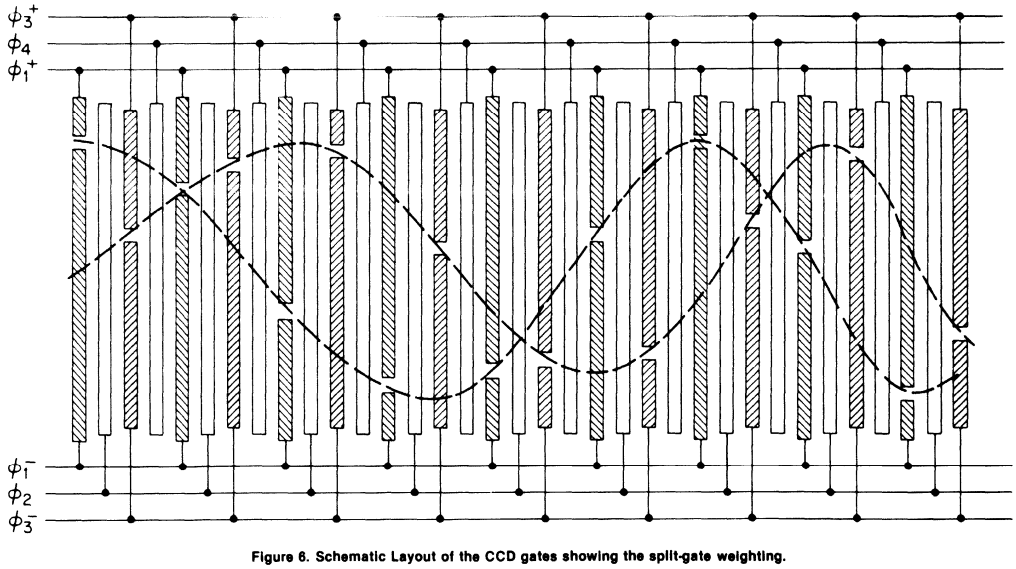


Figure 6. Schematic Layout of the CCD gates showing the split-gate weighting.

5

electrode output techniques to give maximum linearity and dynamic range for this device. In particular, the input structure is designed to compensate for the non-linear effects of the depletion capacitance under the CCD gates of the filter.

Pins 10 and 13 are test points. Each should be connected to a 10K ohm resistor which is connected to the substrate voltage. These pins provide the delayed value of the input signal during testing procedures.

The Transform Algorithm

The complete Discrete Fourier Transform (DFT) is given by the formula:

$$F_k = \sum_{n=0}^{N-1} f_n e^{-i2\pi nk/N}, k = 0, 1, 2 \ldots N-1 \quad (1)$$

where either or both F_k and f_n may be complex. The factor 2nk in the exponent can be replaced by its seemingly more complicated equivalent:

$$2nk = n^2 + k^2 - (k-n)^2 \quad (2)$$

This substitution changes Eq. 1 to Eq. 3 below, where the pertinent factors have been segregated to emphasize the important operations.

$$F_k = e^{-i\pi k^2/N} \sum_{n=0}^{N-1} \underbrace{(f_n e^{-i\pi n^2/N})}_{g_n} e^{i\pi(k-n)^2/N} \quad (3)$$

There are three operations in Eq. 3

1. Multiply each corresponding term of the input discrete-time series, f_n, by the complex factor, exponential $(-i\pi n^2/N)$; that is, by the pair of factors $\cos\pi n^2/N$ and $-i \sin\pi n^2/N$, to produce the combination term in parentheses. Let this new complex sequence be called g_n.
2. Perform a discrete convolution between the sequence g_n and the sequence $e^{+i\pi n/N}$; this is the portion within the summation.
3. Multiply the resulting output sequence by the final factor $e^{-i\pi k^2/N}$ for each point of F_k.

These three operations are indicated in the block diagram of Figure 7, which shows the convolution portion within the dash-line rectangle. For spectral density, outputs from the convolution filter are squared and summed; for obtaining the complete Fourier coefficients, the post multiplier shown at the right in Figure 7 must be provided in place of the squaring function. For a 512-point transform, the convolution portion requires a minimum of 2048 multiplications and 2048 additions for each F_k; it thus represents the bulk of the computational task. It is this portion which is performed by the R5601A convolution filter.

Note that complex multiplication and complex convolution are linear operations; that is, operation on a sum is the same as the sum of the results of separate operations on the members of the sum. Thus, these operations can be broken into corresponding real and imaginary (quadrature) components. Note further that these operations can be handled by real operations, but in separate real and quadrature (imaginary) channels. Thus

$$x \bullet y = (x_R + ix_I) \bullet (y_R + iy_I) =$$
$$(x_Ry_R - x_Iy_I) + i(x_Ry_I + x_Iy_R) \quad (3a)$$

$$x * y = (x_R * y_R - x_I * y_I) + i(x_R * y_I + x_I * y_R) \text{ and}$$

$$(x \bullet y) * z = [(x_Ry_R - x_Iy_I) * z_R - (x_Ry_I + x_Iy_R) * z_I] + i$$
$$[(x_Ry_R - x_Iy_I) * z_I + (x_Ry_I + x_Iy_R) * z_R] \quad (3b)$$

These are the operations indicated in Figure 7 and Eq. 3 where **x** is the signal, **y** is the chirp multiplier and **z** is the convolution portion suppled by the R5601A.

A general, complex input, which has separate real and imaginary (quadrature) inputs, uses the four premultipliers shown at the left in Figure 7, and a single (complex) Fourier coefficient is obtained for each frequency component of the input. The usable input frequency band is from zero to the sample frequency, without ambiguity, because each input sample has two components (that is, there are effectively 2 f_{sample} values per second, and the Nyquist criterion thus allows a band to f_s without aliasing). Another way of viewing these results is to observe that the input premultiplier, with real and quadrature inputs, forms a single-sideband chirp modulator, so that only a single frequency occurs in the chirp input to the filter for each component of the signal.

In most cases, however, inputs are real, the imaginary input is identically zero, and two of the multipliers may be deleted. This (real) signal is simply split into two paths. The signal in one path is multiplied by a cosine chirp $(\cos\pi n^2/N)$ and fed to the real channel of the filter input; the signal in the second path is multiplied by a negative sine chirp $(-\sin\pi n^2/N)$ and fed to the imaginary (quadrature) channel. Each real input component, however, is composed of two complex components, one with positive frequency and one negative frequency. For example, a real signal, $f_n = \cos 2\pi mnT$, is composed of two complex components, $1/2e^{i2\pi mnT}$ and $1/2e^{-i2\pi mnT}$, whose imaginary portions cancel. These two components generate sum and difference chirp frequencies, and for every real signal in the band 0 to $f_{sample}/2$ the negative-frequency component turns up in the band f_{sample} to $f_{sample}/2$ as an alias, thus restricting the useful input band to components lying below this Nyquist limit $f_{sample}/2$. That is, a single input, without the quadrature component results in double-sideband modulation corresponding to both positive and negative frequency components.

The operations above will perform the complete DFT, but to do so requires careful attention to the total operation. In many cases, however, only the magnitude of the power spectrum is required (no phase information), and considerable simplification is possible. First, only the squared magnitude of the various F_k is required, so

$$\left| F_k \right|^2 = \left| \sum_{n=0}^{N-1} (f_n e^{-i\pi n^2/N}) e^{i\pi(k-n)^2/N} \right|^2 \quad (4)$$

The final phase multiplier term, $e^{-i\pi k^2/N}$, may be deleted because it has unit magnitude and does not affect the amplitude. Second, it is possible to operate in a continuous fashion with only slight approximation, because so many points are involved. We step the input data each time a new spectral component is calculated. For a periodic waveform, the principal effect is a slight phase factor which has minimal effect on the result. Equation (4) then becomes:

$$\left| F_k{}^s \right|^2 = \left| \sum_{n=0}^{N-1} (f_n + k e^{-i\pi n^2/N}) \, e^{i\pi(k-n^2/N} \right|^2 \qquad (5)$$

where the designation $F_k s$ indicates a sliding (or continuous) chirp Z transform (2). The chirp-Z designation arises because of the frequency factors $e^{i\pi n2/N}$ which effectively change frequency linearly through the interval $O \leqslant n < N$. The phase and frequency are, respectively:

$$\left| \theta \right| = \pi n^2/N \text{ radians}$$

$$\left| \omega n \right| = \left| d\theta/dn \right| = 2\pi n/N \text{ radians/step}$$

For real inputs then, only one (common) input is used. Further, each filter pair gives one component of a complex number, so for the spectrum analyzer implementation, each component is squared, then added to the other to give the overall squared magnitude or power density.

To see how the convolver-filters work, consider the chirped waveform of Figure 8 where the cosine chirp is

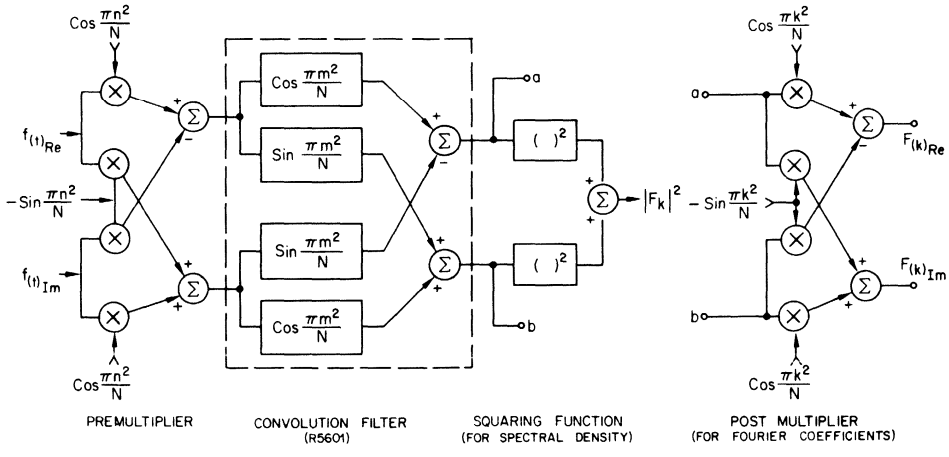


Figure 7. Block Diagram of Implementation of DFT or Spectral Density.

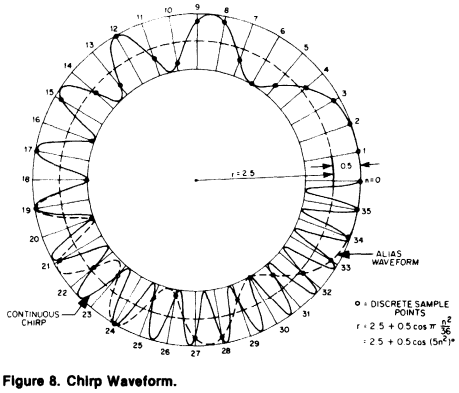


Figure 8. Chirp Waveform.

plotted around the circumference of a circle to emphasize the repetitive nature of the chirp. The "axis" would be a circle midway between the inner and outer circular limits.

Only the cosine chirp is shown in the plot for clarity. Its equation is:

$$r_{cos} = 2.5 + 0.5 \cos \pi n^2/36$$

where n = 0, 1, 2. . . . .36 and where r = 2.5 is the "axis" of the waveform. (For the figure, N = 36, to keep the figure simple, in the R5601A, N = 512.) Note that the waveform is accurate for $0 \leqslant n < N/2$, and thereafter aliasing makes the discrete points also lie on a mirror image of the first 18 points, as shown dotted, whereas the continuous chirp curve has constantly increasing frequency with more alternations, as shown by the solid waveform.

Now consider a dc input. Multiplication by the input chirp weighting produces time samples exactly like

those of Figure 8. These samples are fed into the delay line of the convolver-filters. At the end of 512 clock periods, the samples in the filter exactly match the filter, and the output is maximum at this instant in time (the zero-frequency position).

Next, consider a fixed low-frequency cosine input whose samples are f(t) = cos2πn mn/N, with m an arbitrary (small) factor. This input is multiplied, point by point, with the cosine and sine chirps to give corresponding outputs to the filter channels of

$$P = \cos(^2\pi mn/N)\cos(\pi n^2/N)$$

$$= 1/2\left[\cos\frac{\pi}{N}(n^2 + 2mn) + \cos\frac{\pi}{N}(n^2 - 2mn)\right]$$

$$Q = \cos(^2\pi mn/N)\sin(\pi n^2/N)$$

$$= 1/2\left[\sin\frac{\pi}{N}(n^2 + 2mn) + \sin\frac{\pi}{N}(n^2 - 2mn)\right]$$

These outputs themselves are chirped sum and difference frequencies just like those in Figure 8 except rotated forward or backward by the shift in frequency. Thus, we see that there will be a new time slot, relatively earlier or later than that for dc, where the samples exactly match the filter to give maximum output. At any other position more than a small fraction of a time slot away, the match grows rapidly worse to give essentially zero output when all the weighted samples are added. Note that there is a pair of response from the filter, corresponding to the sum and difference frequencies, since forward rotation corresponds to the sum, and rearward rotation corresponds to the difference, and matches occur due to the symmetry of the (sampled) pattern. As the input frequency is increased, the two responses move toward each other until they meet for an input at the Nyquist frequency of $f_{sample}/2$. There are thus 256 time slots where discrete frequency components can have convolution maxima, with frequency components distributed between dc and the Nyquist frequency. The resolution thus is dependent on the number of points in the matched filters. So if we have 512 point and 100 KHz sample frequency, we would end up with approximately 200 Hz resolution; with 10 KHz sample frequency we would have 20 Hz resolution. However, it should be noted that a frequency midway between adjacent resolution cells spreads its energy approximately equally between the cells; in either event the area under the response tends to remain constant. Windowing, and inputs non-synchronous with the sample rate also tend to spread the spectrum and cause it to vary in amplitude with time.

Why are there four matched filters? Equation (3b) indicated why. Even if the input is purely real (i.e., $x_I = 0$), the correlation process still requires all four components of z: two in the real channel and two in the imaginary channel to permit arbitrary phase. Qualitatively, for example, while a real, even input correlates primarily with the cosine chirp, any odd components (of different phase) require the sine chirp filters. For general signals, each filter section contributes appropriately to the correlation.

Specifications and Performance

The diagram of Figure 4 indicates, in part, the configuration and drive requirements of the R5601A. Typical operating conditions are indicated in Table II. Input impedances to the various gates are principally capacitive in nature. The delay-line outputs are connections to active FET sources of the output source followers, so these outputs normally are connected through load resistances (approx. 10K ohm) to the substrate potential. These delay-line outputs are normally used only during testing and initial adjustment. The delayed signal appears superposed on clock pedestals as in Figure 9, where the cross-hatched portion represents variable values, depending on the particular signal sample. If the viewing oscilloscope sweep is synchronized to an input sinusoidal signal, the output should show a stair-step approximation to the input when biases, etc., are correctly adjusted.

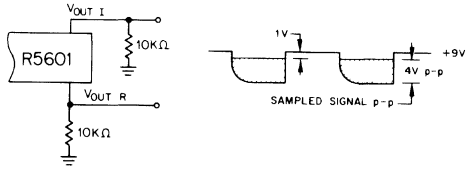


Figure 9. Illustration of the Delayed Sampled Output, V_{OR} or V_{OI}, used for test purposes.

Evaluation Module

A printed-circuit evaluation module is available from Reticon. This module provides the external functions of clock drive, premultipliers, output buffers, squaring circuits, etc., to implement a spectral-density evaluator for real inputs. It is self-contained except for power supplies. Its design is a compromise between performance and cost, making it useful principally for initial evaluation and simple spectral analysis. Its nominal sample rate is 100 KHz but an external input permits sampling at lower rates if desired. Further details may be found in specification data for the RC-5601 Evaluation Board.

References

(1) "The Chirp Z-Transform Algorithm", L. R. Rabiner, R. W. Schafer, and C. M. Rader; IEEE Transactions Audio Electroacoust, Vol. AU-17, pp. 86-92, June 1969.

(2) "A 500-Stage CCD Transversal Filter for Spectral Analysis", R. W. Broderson, C. R. Hews, and D. D. Buss; IEEE Journal of Solid-State Circuits, SC-11 No. 1 (February 1976) pp, 75-84.

(3) "The Fast Fourier Transform's Errors Are Predictable, Therefore Manageable", R. W. Ramirez; Electronics, Vol. 47, No. 12, June 13, 1974, pp. 96-102.

Table I
R5601A Pin Functions

Pin No.	Designation	Function
1	V_{sub}	Substrate
2	ϕ_4	Minor clock for CCD transport
3	COM	Common (ground) connection
4	ϕ_1^-	(-) weights of ϕ_1 split-electrode gates
5	ϕ_{rl}	Reset gate for ϕ_1 split-electrodes
6	ϕ_1^+	(+) weights of ϕ_1 split-electrode gates
7	I_{SGR}	Input sampling gate, real channel
8	I_{RGR}	Input receiving gate, real channel
9	Input real	Signal input, real channel
10	V_{OR}	Delay-line output, real channel
11	Reset	Delay-line output reset control
12	V_{OG}	Delay-line output control gate bias
13	V_{OI}	Delay-line output, imaginary channel
14	Input Imaginary	Signal input, imaginary channel
15	I_{RGI}	Input receiving gate, imaginary channel
16	I_{SGI}	Input sampling gate, imaginary channel
17	ϕ_3^+	(+) weights of $\phi_1$split-electrode gates
18	ϕ_{r3}	Reset gate for ϕ_3 split-electrodes
19	ϕ_3^-	(-) weights of ϕ_3 split-electrode gates
20	V_{DD}	Drain supply for source-follower buffers
21	ϕ_2	Minor clock for CCD transport
22	V_{CB}	Delay-line corner-control-gate bias

Table II
Definitions and Electrical Specifications

Pin No.	Functions	Symbol	Min	Typ	Max	Units	Note
1	Substrate	Sub	0	-1.2	-7	volts dc	3,5
2	Minor phase clock	ϕ_4	5	6	7	p-pvolts	1,4
3	Common	Comm	—	—	—	—	2
4	Major phase clock & Signal Output Line for Minus Signal	ϕ_1^-	10	12	14	p-p volts	1,4
5	Reset gate for ϕ_1 clock line	ϕ_{rl}	5	15	22	p-p volts	1,4
6	Major phase clock and Signal Output Line for Positive Signal	ϕ_1^+	10	12	14	p-p volts	1,4
7	Input sampling gate, real	I_{SGR}	10	15	22	p-p volts	1,4
8	Input receiving gate, real	I_{RGR}	$0.5I_{SGR}$	$0.75I_{SGR}$	I_{SGR}	volts dc	5
9	Signal input, real	IN-Re	6	9	11	volts dc (bias)	
10	Delayed output, real	V_{OR}		see text			
11	Reset input to Channel Output Amplifier	RESET	10	15	22	p-p volts	1
12	Signal Channel Output Gate	V_{OG}	2	3	5	volts dc	5
13	Delayed Output, Imaginary	V_{OI}		see text			
14	Signal Input, Imaginary	IN-Im	6	9	11	volts dc (bias)	
15	Receiving Gate, Imaginary	I_{RGLI}	$0.5I_{SGIL}$	$0.75I_{SGI}$	I_{SGI}	volts dc	5
16	Input Sampling Gate, Imaginary	I_{SGI}	10	15	22	p-p volts	1
17	Major Phase Clock and Signal Output Line for Positive Signal	ϕ_3^+	10	12	14	p-p volts	1,4
18	Reset clock for ϕ_3 clock line	ϕ_{r3}	5	15	22	p-p volts	1,4
19	Major Phase Clock & Signal Output Line for Minus Signal	ϕ_3^-	10	12	14	p-p volts	1,4
20	Supply Voltage for output	V_{DD}	8	15	22	volt dc	1,5
21	Minor phase clock	ϕ_2	5	6	7	p-p volts	1
22	Corner bias	V_{CB}	2	3	5	volts dc	1,5

NOTE: 1. All clocks swing from 0 to 0.4 volts low to a high as specified.

2. Common is reference level for all voltage measurements and is normally grounded.

3. The substrate must be at lowest potential, normally -1.2 volts.

4. See figure for clock waveform and timing; note that all waveforms must be free from over and under shoots with edges as clean as possible.

5. These are bias input nodes and must be well bypassed.

Table II (cont'd)
Specifications (25°C)

INPUTS			
Signal Inputs	**Symbol**	**Typical**	**Units**
Bias Level	Input Real	9	volts
Signal Level	Input Imaginary	3-4	volts (p-p)
Input Capacitance		5	pf
Clock & Drive			
Split-Electrode Clock Amplitude (Applied to Capacitors, See Figure 2)	ϕ_1, ϕ_3	30	volts
Electrode Clock Amplitude	ϕ_2, ϕ_4	4-6	volts
Reset Clock Amplitude	ϕ_{R1}, ϕ_{R3} Reset	12-15	volts
Clock Line Capacitance	ϕ_2, ϕ_4	200	pf
Clock/Sense Line Capacitance	ϕ_1, ϕ_3	500	pf
Minimum Sample Rate		4	KHz
Maximum Sample Rate		2	KHz
Drain Supply	V_{DD}	15	volts
Output Gate	V_{OG}	3	volts
Corner Gate	V_{CG}	3	volts
Substrate Bias	V_{sub}	-1.2	volts
Power Dissipation	—	.5	watts
OUTPUTS (ϕ_1^+, ϕ_1^-, ϕ_3^-, ϕ_3^+)			
Signal Level (Superimposed on Clock Level)		.5	volts (p-p)
PERFORMANCE			
Dynamic Range (Peak signal to RMS noise)		60	dB
Linearity (Total harmonic distortion)		1	%
Tap weight Accuracy		8 bits	plus sign

The weighting coefficients for these two devices are:

R5601A-1 $\quad \begin{Bmatrix} \cos \\ \sin \end{Bmatrix} \left\{ \frac{\pi (n-1)^2}{512} \right\}$ $\quad$ Tap Number = n, $1 \leq n \leq 512$

R5601A-2 $\quad \begin{Bmatrix} \cos \\ \sin \end{Bmatrix} \left\{ \frac{\pi (n-257)^2}{512} \right\} \cdot \left\{ 1/2 \left[1 - \cos \left(\frac{2\pi (n-1)}{511} \right) \right] \right\} \quad 1 \leq n \leq 512$

(Chirp Weighting) $\qquad$ (Window Function)

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DESCRIPTION

The R5602 transversal filter family includes four standard filter responses. Each design is a monolithic 64-tap delay line with the finite impulse response or weighting defined by the relative sizes of split electrodes in the device. Custom filter designs are possible with a single mask change.

Sample rates from 1KHz to 1MHz allow a wide range over which the user may "tune" the filter response by simply changing the external trigger frequency.The transversal filter is unique in that filter cutoff rates exceed 150 dB/octave while preserving linear phase response in the passband. This is important in reduction of pulse distortion for telemetry signals, and a minimization of overshoot in the step response.

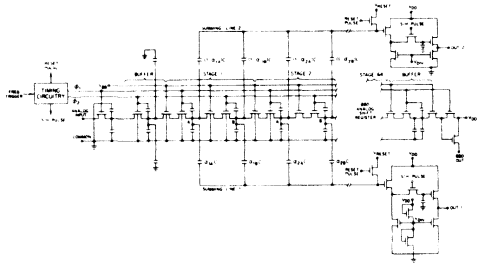
TYPICAL APPLICATIONS

- Telemetry and Modems with PSK, QPSK, FM & FSK Formats
- Anti-Alias Filter for Data Acquisition Systems
- Tracking/Programmable Filter
- Matched Filter/Fixed Correlator
- Real-Time 64-Point Discrete Fourier Transforms via the Chirp-Z Transform
- Pulse Compression

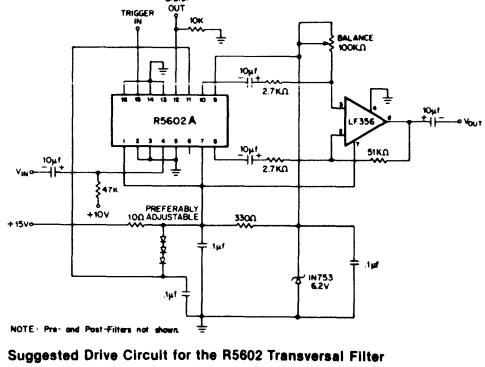
DEVICE OPERATION

The sample rate is controlled by $\varnothing_1$ at one-fourth the clock trigger frequency. At the negative transitions of $\varnothing_1$, new samples of the input waveform are entered (locked) into the charge-transfer device (CTD), which are clocked along the bucket-brigade delay line (BBD).

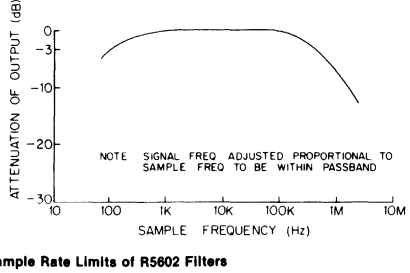
For test purposes, the unfiltered but buffered output of the delay line is accessible at BBD OUT, delayed from the input by 65 sample periods.



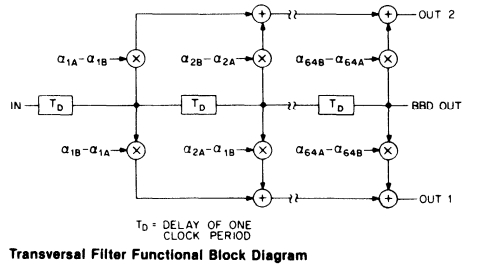
R5602 Transversal Filter Equivalent Circuit



Suggested Drive Circuit for the R5602 Transversal Filter



Sample Rate Limits of R5602 Filters



Transversal Filter Functional Block Diagram

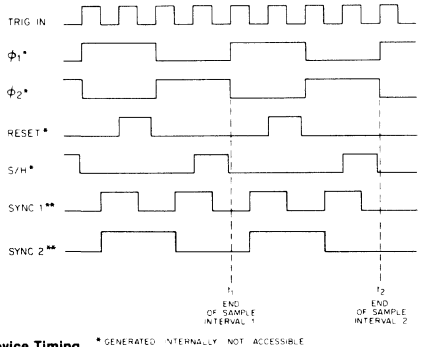
The spectral characteristic depends on the sample frequency; thus, the frequency characteristic may be shifted merely by shifting the sample frequency. At the extremes, the sample frequency is limited as shown above. At the low end, the filter performance degrades due to leakage; at the high end due to limitations of the on-chip timing circuitry.

The maximum useable input signal is limited by the tolerable harmonic distortion.

Linearity, in general, increases as signal amplitudes are reduced. Thus, an improved harmonic-distortion ratio may be obtained by reducing signal amplitude, but at the expense of reduced dynamic range.

CASCADE OR PARALLEL OPERATION

To cascade two or more transversal filters requires a parallel connection of the trigger signal pins (pin 15). For synchronized parallel clocking, sync 1, sync 2, and the trigger line (pin 16) must be clocked with the waveforms shown below. The sync waveforms can be derived from the trigger clock with a flip flop and level shifted to the specified value.



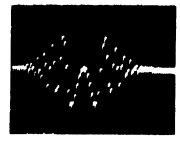
Device Timing * GENERATED INTERNALLY, NOT ACCESSIBLE
** MUST BE GENERATED EXTERNALLY AND APPLIED FOR CASCADE OR PARALLEL SYNCHRONIZATION OF TWO OR MORE FILTERS

STANDARD FILTERS

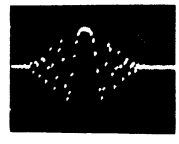
The pre-programmed types are:
R5602-1 Narrow Lowpass
-3 Narrow Bandpass
-7 Sine Chirp } Hanning
-8 Cosine Chirp } Windowed

SPECIAL FUNCTION DEVICES

The -7 and -8 versions of the R5602 filter family have impulse responses corresponding to a sin or cos chirp with the Hanning window. These devices can be used to implement a 64 point chirp-z transform, or they can perform pulse compression of chirp waveforms such as used in sonar and radar. For a particular application, Reticon can provide applications assistance.



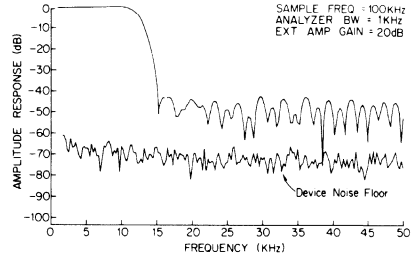
R5602-7 windowed SIN Chirp Impulse Response.



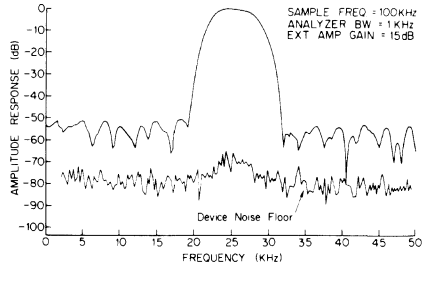
R5602-8 windowed COS Chirp Impulse Response.

CUSTOM FILTERS

Low cost customized filter responses are made possible by modification of a single mask used in device fabrication. Requests for custom responses can be submitted as either a desired frequency response or a desired impulse response.

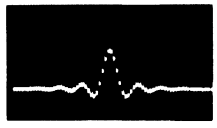


R5602-1 Narrow Lowpass Filter Spectral Response



R5602-3 Narrow Bandpass Filter Spectral Response

FILTER IMPULSE RESPONSES



R5602-1 Narrow Lowpass

R5602-3 Narrow Bandpass

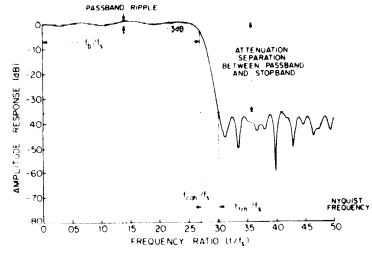


Illustration of Frequency Characteristic Definitions, Lowpass Filter.

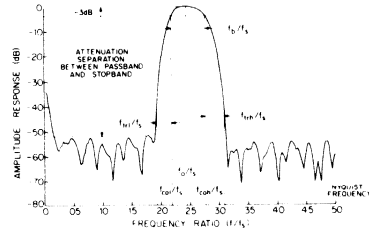


Illustration of Frequency Characteristic Definitions, Bandpass Filter.

TABLE 1. R5602 FILTER PERFORMANCE (TYPICAL)

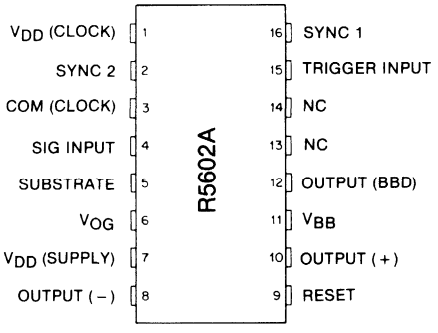
PARAMETER @25°C.	Lowpass R5602-1 narrow	Bandpass R5602-3 narrow
Center Frequency f_o/f_s(1)		.25
Bandwidth f_b/f_s	.12	.055
Low cutoff frequency f_{col}/f_s		.222
High cutoff frequency width f_{coh}/f_s	.125	.275
Low transition width f_{trl}/f_s		.03
High transition width f_{trh}/f_s	.025	.035
Separation between passband and stopband in dB	42	50.9
Rollup rate in dB/octave		271
Rolloff rate in dB/octave	185	291
Harmonic distortion for $1V_{pp}$ input signal in dB(2)	-55	-55
Harmonic distortion for $3V_{pp}$ input signal in dB	-40	-40
Dynamic range for $3V_{pp}$ input signal in dB	63	65
Dynamic range for $1V_{pp}$ input signal in dB	53	55
Insertion loss in dB	20	15
Shape Factor	1.2	2.2
Max. ripple in passband portion in dB	.2	.2

(1) f_s is the internal sample frequency = 1/4 (external trigger clock frequency)

(2) OdB = 1 V_{pp}

TABLE 2. SPECIFICATIONS

ABSOLUTE MAXIMUM RATING	MIN		MAX	UNITS
Voltage on any terminal with respect to common	-0.4		+ 20	V
Storage Temperature	-55		+ 125	°C
Temperature under bias	-55		+ 85	°C
DRIVE REQUIREMENTS	**MIN**	**TYP**	**MAX**	**UNITS**
Trigger Amplitude	4.6	10	17	V
Trigger Frequency	.004		4	MHz
Sample Frequency	1/4 of Trigger Frequency (internally generated)			
Sync Amplitude	10		V_{DD}	V
Trigger Input Capacitance		10		pF
V_{DD}	14	15	16	V
V_{BB}		V_{DD}-2		V
V_{reset}	5	6	8	V
DC Power Dissipation		180		mW
INPUT/OUTPUT				
Input DC Bias		10-11		V
Input Signal Amplitude		1	3	Vpp
Input Capacitance at 5 Volts:		7		pF
Input Impedance (at f_s = 100 KHz)		30K		Ω
Dynamic Range		See Table 1.		
Output Impedance		1.2		kΩ



Dual-In-Line Package

WARNING: Damage to the device may result if the input terminal is a.c. coupled. When the power is removed from the device while signal is applied to input terminal, the substrate may become biased in the forward direction causing the input gate protection to "short circuit."

TABLE 3. PIN CONNECTIONS

Pin	Function	Suggested Voltage/Signal Connection
1	V_{DD} (clock	+ 15V
2	Sync 2	Common
3	Clock Common	Common
4	Signal In	Signal
5	Substrate	Common
6	V_{OG}	N/C or 5-10V if BBD out is used
7	V_{DD} (Signal)	+ 15
8	$V_{out}1$	− Input of differential amplifier
9	V_{reset}	10μf cap to common
10	$V_{out}2$	+ Input of differential amplifier
11	V_{BB}	+ 13/14V
12	BBD Out	100K ohm to common
13	NC	Common
14	NC	Common
15	Trigger In	Clock at 4 times sample frequency; amplitude 10V
16	Sync 1	Common

Dynamic range is defined as:

$$\text{Dynamic range} = 20 \log \frac{V_{in}{}^{rms\ max}}{V_{noise}{}^{rms}}$$

Insertion loss is defined as:

$$\text{Insertion loss} = 20 \log \frac{V_{out}{}^{p\text{-}p}}{V_{in}{}^{p\text{-}p}}$$

The Shape factor is defined as:

For the lowpass filter,

$$\text{Shape factor} = \frac{\text{Attenuation bandwidth at -40 dB}}{\text{3dB bandwidth}} = 1 + \frac{f_{trh}}{1 + f_{coh}}$$

For the bandpass filter,

$$\text{Shape factor} = \frac{\text{Attenuation bandwidth at -40 dB}}{\text{3dB bandwidth}} = 1 + \frac{f_{trl} + f_{trh}}{\Delta f}$$

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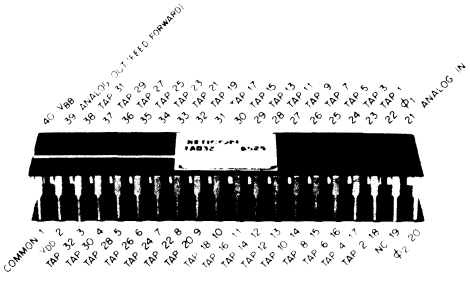
EG&G RETICON TAD-32 TAPPED ANALOG DELAY



KEY FEATURES

- **Monolithic construction**
- **Full wave output from each tap**
- **32 equally spaced taps, with separate feed-forward tap**
- **Buffered outputs from each tap**
- **Tap delay linearly variable with clock period**
- **Sampling rates to 5 MHz**
- **40 db passband-to-stopband ratio (as a filter)**
- **60 db dynamic range**
- **Simple I/O and clock circuit**
- **Low power dissipation**
- **40-pin dual-in-line package**

The Reticon TAD-32 is a tapped analog delay line fabricated with the most advanced n-channel silicon-gate integrated-circuit technology. It consists of a charge-transfer device with 32 taps equally spaced one sample-time apart along the device. It is designed specifically for use in the realization of transversal filters, but it likewise is applicable to recursive or other filter types. Typical applications include: low pass filters, band pass filters, matched filters, phase equalizers, phase shifters, tone generators, function generators, correlators, and simple tapped delays.

GENERAL DESCRIPTION

TAD-32 is a 32-stage charge-transfer device which permits the storage of analog signals with recovery of the signals at multiple separate outputs at successive delay times later. The taps on each stage are brought to the outside through buffer amplifiers. Each buffer amplifier output appears as a source follower, thus permitting variable loading of the taps in order to create various tap-weight functions. The taps are spaced one sample time apart along the delay. An additional special feed-forward output tap is provided so that multiple devices may be cascaded without causing discontinuity in the spacing of the taps from one device to the next. With this arrangement, timing integrity is maintained. The ability to cascade devices permits the user to build processors (such as transversal filters) with more than 32 taps.

DEVICE OPERATION

The equivalent circuit is shown in Fig. 1. Samples are set up on the initial storage node during the time period when the $\emptyset_1$ clock waveform is at its high (positive) level. When $\emptyset_1$ drops, the sample value is frozen and the simultaneous rise of $\emptyset_2$ permits exchange of charge with the tap-1 node; similarly for other nodes. The sample values thus first appear at the various tap outputs when $\emptyset_2$ rises. When $\emptyset_2$ falls and $\emptyset_1$ rises, the charge state is transferred to the second node for each tap. The paralleling of the buffer outputs thus maintains the output value at the tap for both halves of the clock period. The resulting output is a full-wave (or full-period) output. Further, there is one sample time delay between the samples as they appear at successive output taps. The last node supplies a feed-forward tap at the proper time to provide the set-up signal for another, series-connected TAD-32, so that multiple-section processors with more than 32 taps can be implemented. Clocking of the second device must be synchronous with the first, i.e., $\emptyset_{1A} = \emptyset_{1B}$.

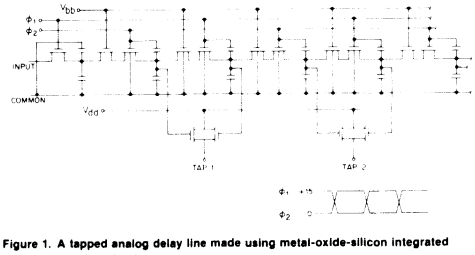


Figure 1. A tapped analog delay line made using metal-oxide-silicon integrated circuit technology.

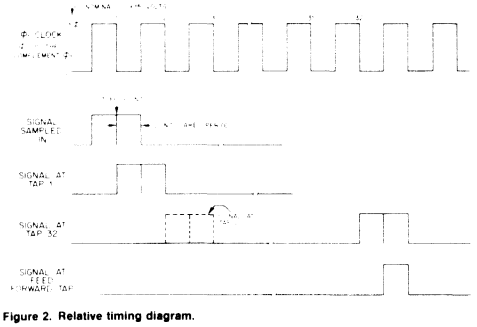


Figure 2. Relative timing diagram.

The device is capable of sampling rates from below 1KHz to more than 5 MHz. This capability permits the translation of a given filter characteristic over a range of more than three orders of magnitude in frequency simply by varying the clock rate. A two-phase complementary square-wave clock with amplitude in the range of 12 to 15 volts is required to drive the device. The clock phases are positive square waves, as shown in the inset of Fig. 1 and in more detail in Fig. 2. The clocks drive the nodes positive, thus providing a positive output with reference to ground at each tap. The output from each tap is a full-wave or boxcar output, as discussed above; no additional filtering is necessary before summing with the desired weights. The summing amplifiers can combine the summing and filtering functions.

5

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FUNCTIONAL PERFORMANCE

The TAD-32 functions as a discrete-time processor. Time is quantized, but signal amplitudes retain the analog values associated with the discrete-time values corresponding to the falling edges of $\emptyset_1$ (the sample times). Behavior is that of a discrete-time or sampled-data system. The specifications and performance data thus must be interpreted in the light of such a system. An indication of the performance is given in Figs. 3 and 4 for the simple equal-tap-weight case.

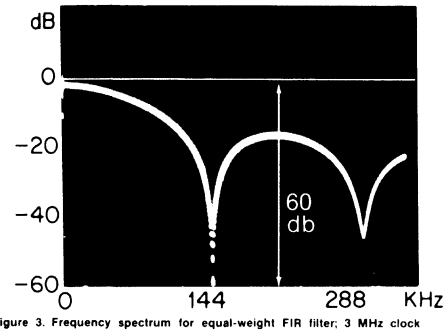


Figure 3. Frequency spectrum for equal-weight FIR filter; 3 MHz clock frequency, 3 Hz resolution bandwidth, 360 KHz scan. (Note the 60-db dynamic range as shown by the null depth.)

1. Example of Performance

The simplest form of a low-pass filter has all taps weighted equally and summed. For this equal-weight transversal filter, the frequency response is as shown in Fig. 3 above. The impulse response, which bears a unique relationship to the frequency response, is shown in Fig. 4. Filter design may be based on a desired frequency response, but generally proceeds by first finding the impulse response corresponding to the frequency response.

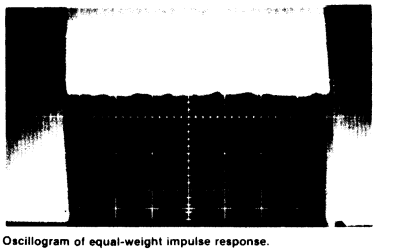


Figure 4. Oscillogram of equal-weight impulse response.

For the case of Fig. 4, a single (unit-weight) sample is provided as input. This sample then appears once at each tap output, then moves to the next, and finally out of the system. Thus, the summed tap outputs is a string of 32 successive unit-amplitude segments as in Fig. 4. The frequency response for this case is ideally $\sin(32\pi f_S/f_C)/\sin(\pi f_S/f_C)$, where f_S is the signal frequency and f_C the sample frequency. The spectrum of Fig. 3 shows this pattern with a 60-db null depth. The resolution bandwidth was 3 Hz and the frequency scan 0 to 360 KHz. A careful plot of data derived from Fig. 3 is indistinguishable from the theoretical response.

It is obvious that the equal-tap-weight described in Example 1 gives a form of low-pass filtering. However, the filter is far from ideal even with perfect performance. Side lobes are large, and the general stop-band performance is poor. A basic improvement is described in Example 2.

2. Example of tap-weight tailoring for improved performance

The difficulty with the filter of Example 1 lies in the very simplicity of the tap weights. As illustration, suppose we postulate an "ideal" rectangular passband. Such a passband requires an impulse response approximating a sin x/x form, extending over all time. Since, however, such an "ideal" response is impractical to achieve, we modify the sin x/x function by multiplying tap weight values by a Hamming window[1] weighting function. This gives major weight to central taps and diminishing weight to outer taps, decreasing to zero where we run out of taps because of finite limitations on the possible number. Such a weighting, for 16 taps between zero crossings of the weighted sin x/x function, is shown in Fig. 5 as a calculated oscilloscope overlay. An actual measured impulse response corresponding to this weighting is shown in Fig. 6, and the frequency response, measured with a spectrum analyzer of 1 KHz resolution bandwidth, is shown in Fig. 7. Further details of the measurements and design procedure may be found in Refs. 1 and 2. For Figs. 6 and 7, tap weights were initially selected to 1%, then the major taps slightly altered by simply adjusting the tap weights until the actual output best approximates the desired pattern overlaid on the face of the oscilloscope (see Fig. 5).

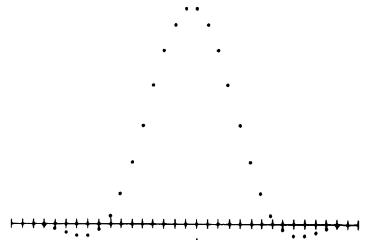


Figure 5. Oscilloscope overlay for Hamming-windowed sin x/x impulse response, 16 taps between zero crossings.,

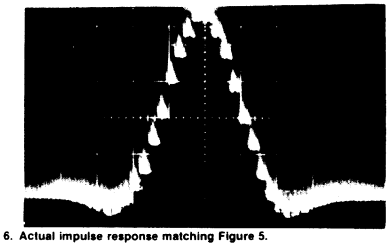


Figure 6. Actual impulse response matching Figure 5.

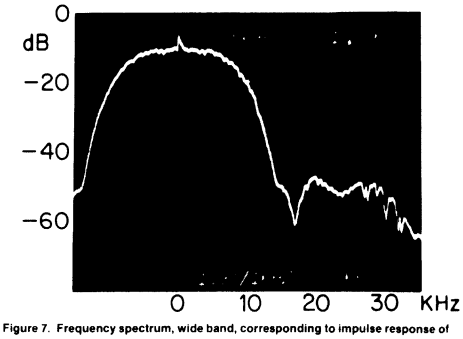


Figure 7. Frequency spectrum, wide band, corresponding to impulse response of Figure 6.

DYNAMIC RANGE

The usable dynamic range normally exceeds 60 db, as shown in Figs. 3 and 8. The data were taken on a spectrum analyzer, which provided the required filtering against clock noise, while retaining any spurious or harmonic responses, as well as showing the noise floor. In any normal application, adequate input and output filtering are an integral part of the design. The input filter is required to prevent aliasing responses, the output filter to separate base-band components from the clock-frequency components (and harmonics). The latter also serves to smooth the full-period boxcar variation of the individual or summed outputs so as to recover the base-band components. The dynamic-range measurements of Fig. 8 are applicable to the low-pass filters of the examples.

LINEARITY, DISTORTION, AND NOISE

These attributes of the device give supplemental measures of its performance. For small signals, the relationship between input and output is highly linear. As the signal amplitude increases, slight departure from linearity occurs. Ultimately, an overload limit is reached where a rapid onset of clipping distortion accompanies any further signal increase. The rapid rise of distortion with excessively high signal level is indicated by the data of Fig. 8. The linearity and distortion data are obtained from single-tap measurements.

Noise is of two general types: (a) clock-related noise which can largely be eliminated by appropriate output filtering, and (b) random noise, which arises from statistical charge variations, resistance in transfer paths, and miscellaneous other sources. Without filtering, the clock noise is dominant, but this noise is largely removable by appropriate output filters. The residue after filtering, particularly that within the desired signal band, sets the lower signal limit. On a broadband oscilloscope presentation the tangential noise is more than 40 db below a 4V p-p reference signal. In a 3 KHz filter band, the noise is more than 60 db below the reference signal, as indicated in Fig. 8. This figure shows various measurements taken on a single-tap basis; multiple-tap performance is illustrated by Fig. 3.

As with all solid-state devices, elevated temperature increases background current and hence increases noise. It also modifies slightly the desired bias point, particularly at low clock frequencies where delay is maximum. But because there are only 64 charge transfers per device, the effects are minimal. Performance at very low clocking frequencies is most affected by elevated temperature because of the increased discharging effect of the leakage (background) current. Increasing the temperature increases the leakage and thus increases the minimum sampling frequency by a factor of two for every 7°C increase above normal room temperature.

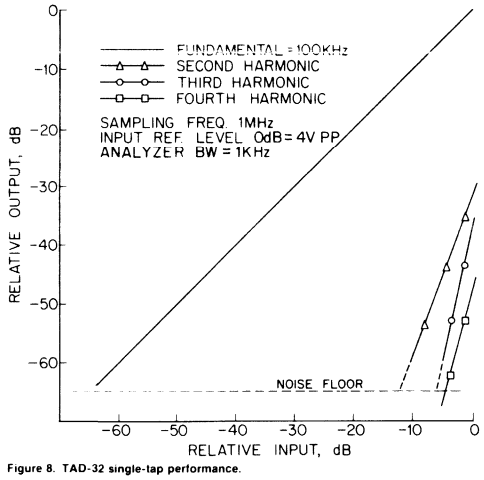


Figure 8. TAD-32 single-tap performance.

FREQUENCY RESPONSE

It should be remembered that the TAD-32 is a sampled-data system. Input signals may be successfully sampled at rates up to 5 MHz. Low-frequency signals are sampled many times per cycle and reproduced at the output without loss. High frequency signals when sampled and reestablished are subject to a $\sin(\pi f_S/f_C)/(\pi f_S/f_C)$ roll off, characteristic of sampled data systems. The device itself introduces negligible attenuation.

DRIVE CIRCUIT

A suitable drive circuit is illustrated in Fig. 9. The Schottky TTL flip-flop converts the input clock (at $2f_C$) into the desired complementary square-wave clock signals at Q and $\overline{Q}$. Rise and fall times are adequately short (less than 20 nsec) and skew is minimal (waveforms cross at the approximate 50% level). The 0026 translator (National or Motorola) converts the amplitude and level to those required by the TAD-32 while preserving the integrity of the waveforms. The output bias and signal summing arrangements have evolved to the circuit shown in Fig. 9 as the best compromise to conflicting requirements. For equal tap weights, the potentiometers are offset by equal amounts (i.e., resistor values to the + line are all equal, as are the complementary values to the - line; a centered potentiometer gives zero tap weight); for other filter arrangements, the ratio of the resistances determines the tap weight. The TC-32A Evaluation Circuit Card incorporates the test circuit shown in Figure 9.

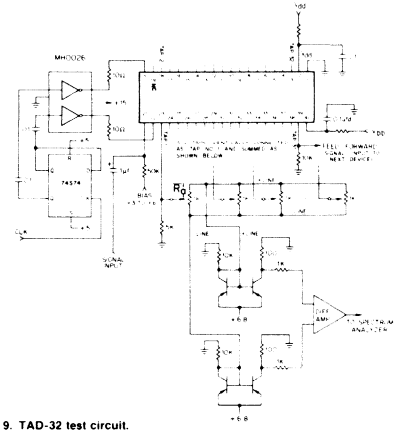


Figure 9. TAD-32 test circuit.

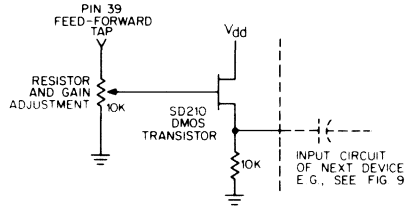


Figure 10. Suggested interface for serial operation. Clocks are synchronous.

To obtain a greater number of taps, devices may be cascaded using synchronous clocks. The feed-forward output of the first device becomes the input to the second device. Figure 9 shows the required arrangements and d-c load on the feed-forward tap — pin 39 — (the latter is needed only when cascading multiple devices). The circuit of Fig. 10 permits an adjustment of gain to unity, and the SD210 source follower provides the requisite buffer to give good high-frequency performance when driving a capacitive load. A bipolar transistor in place of the SD210 is less suitable because of its larger effective input capacitance.

In normal operation, V_{dd} operates at the same level as the clock; V_{bb} is preferably adjusted to a slightly lower potential, in the region of zero to one volt *lower* than the

maximum voltage of the clock. Since, with the 0026, the maximum clock voltage is approximately one diode drop below V_{cd}, an adjustment of V_{bb} approximately one to one and one-half volts below V_{dd} is typical.

Although the clock drive circuit shown is preferred, a CMOS D-type flip-flop, such as the type 4013 (B version preferred), will directly provide complementary clock waveforms which are adequate for many applications.

Note that there are conflicting requirements in the tap output circuit. For linearity and minimization of tap-to-tap crosstalk, it is desirable that the taps see a relatively low a-c impedance; further, d-c coupling is desirable to avoid coupling difficulties at low scan rates. On the other hand, it is desirable that the d-c current level be much less than would flow into a low-resistance path to ground. Further, individual differences in source-follower thresholds, etc. give rise to a tap-to-tap variation which requires relatively low gain until the differential combination has been accomplished. The circuit of Fig. 9 compromises effectively among the above factors. Weighting is adjustable over the range $-1 \leq W \leq +1$ for each tap by adjustment of the ratio of resistances connecting the + line and – line, respectively. Designated as R_a the resistance between the potentiometer slider (Fig. 9) and the positive bus, where $O \leq R_a \leq 1000$ ohms. Then $R_a = 500$ ohms gives the central or zero-weight value, $R_a = O$ gives the maximum positive weight, and $R_a = 1000$ ohms gives the maximum negative weight. The tap weight is then given by $W = (500 - R_a)/500$, or the resistance value by $R_a = 500\ (1-W)$ ohms where W is the tap weight and is $-1 \leq W \leq +1$. Note that resistance values other than 1000 ohms are possible; higher values lead to excessive crosstalk and lower values lead to excessive d-c balance sensitivity.

It is important that an active tap see a low a-c impedance; a potential variation at the tap couples a small charge variation into the next earlier and next later charge packet. In a filter application such crosstalk merely requires slight adjustment of the tap weights, but it is better to avoid the coupling by means of low impedance load. For the same reason, unused taps should either be left floating or, preferably, connected to V_{dd}. They should *not* be loaded or connected to common, both to avoid crosstalk and to avoid dissipation.

TC-32A EVALUATION CIRCUIT CARD

The TC-32A Evaluation Circuit Card incorporates the basic circuit shown in Fig. 9 and is available from RETICON. It provides the required peripheral circuitry including bias, signal buffering, and clock and start waveforms. External interface with timing logic, etc. is at TTL level to assist in functional use of the TAD-32. The board may be incorporated into systems, if desired, and is particularly useful during evaluation and initial system design. A descriptive data sheet is available for the TC-32A. The board is available in three versions, designated by dash numbers (-01), (-02), and (-03).

The (-01) version is standard and has fixed resistors of 800 ohms and 200 ohms in place of the potentiometers of Fig. 9: all weights are of the same polarity.

The (-02) version is the most versatile, with adjustable tap-weight potentiometers as shown in Fig. 9.

The (-03) version is supplied without weighting resistors, so that any customer-desired weighting arrangement may be implemented.

REFERENCES

1. G.P. Weckler: "A Tapped Analog Delay for Sampled Data Signal Processing" (Reticon Technical Note No. 105)
2. R.R. Buss and S.C. Tanaka: "Implementation of Discrete-Time Analog Filter and Processing Systems" (Reticon Technical Note No. 111)
3. U. Strasilla, G.P. Weckler: "Charge Transfer Devices for Sampled-Data Processing" (Reticon Technical Note No. 114)

SPECIFICATIONS (25°C)

Absolute Maximum Rating	**Min.**	**Max.**	**Units**
Voltage on any terminal with respect to common	-0.4	+20	Volts
Storage temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

Drive	**Min.**	**Typical**	**Max.**	**Units**
Clock frequency	0.001		5*	MHz
Clock amplitude, $V_\emptyset$ (Figs. 1, 2)	10	15	16	Volts
Clock line capacitance (each)		50		pf
V_{bb} (optimum)		$V_\emptyset$-1	$V_\emptyset$	Volts
V_{dd}	$V_\emptyset$	+15	16	Volts
DC power dissipation**		200	700	mwatts

*Performance degraded above 2 MHz clock rate.

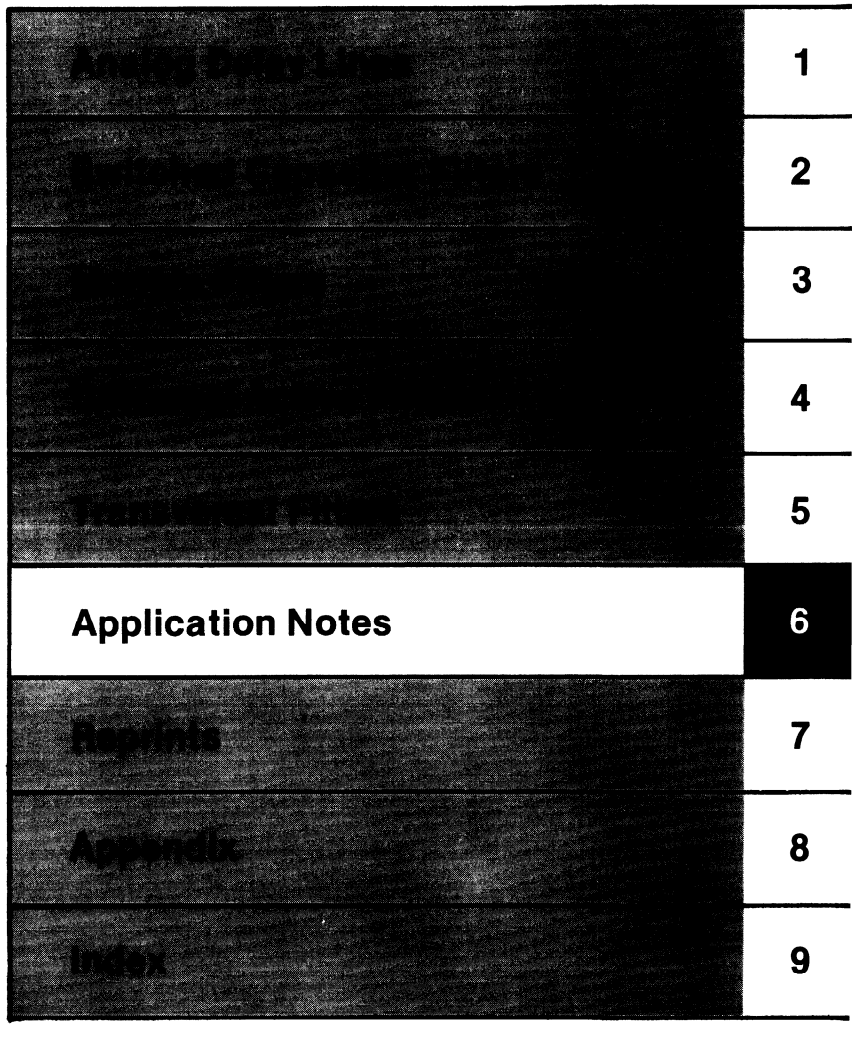
**DC power dissipation is strongly dependent on the number of taps used and on tap load currents. When all 32 taps are used with 10 K ohm loads, typical dissipation is 200 mwatts.

***Optimum bias is dependent on clock and supply voltages.

WARNING: Damage to the device may result if the input terminal is a.c. coupled. When the power is removed from the device while signal is applied to input terminal, the substrate may become biased in the forward direction causing the input gate protection to "short circuit".

Input/Output	**Typical**	**Max.**	**Units**
Input capacitance @ +4 V Bias	8		pf
Output capacitance of each tap @ +5 V Bias	3		pf
Output transconductance (at +5 V level, 10 K Ω d-c load)	1.1		ma/v
Input Bias***	3		Volts
Input signal (p-p)		4	Volts
Tap d-c level	+5		Volts
Unused taps	Connect to V_{dd}		
Performance Characteristics			
A. Single-tap response:			
Dynamic range (See Figs. 3 and 8)	60		db
Linearity (See Fig. 8)			
Harmonic intercepts (See Fig. 8)			
B. 32-tap summed response:			
Dynamic range (See Fig. 3)	60		db
Input sensitivity, S/N ~1	4		mV p-p

Analog Signal Processing Products



MAKING MUSIC WITH CHARGE-TRANSFER DEVICES

ABSTRACT

What is a charge-transfer device and how can it be used to make electronic music?

Charge transfer devices represent a rapidly developing area of semiconductor technology which allows one to controllably delay analog signals. The ability to controllably delay an analog signal permits the realization of filters whose characteristics are also controllable. A "flanger" is a typical example of an electronically variable "comb filter." When applied to percussive instruments it produces a hollow swishy sound akin to that of a jet plane but without the rumble and roar. The flanger, as well as several other applications of analog delays, will be described in more detail later.

Let us first review the fundamentals of charge-transfer devices. The realization of an analog delay, its principles of operation, and its basic characteristics will be reviewed.

FUNDAMENTALS OF CHARGE-TRANSFER DEVICES

"Charge-transfer device" is a generic term which is applied to a family of solid-state electronic components, which under the application of a proper sequence of clock pulses moves packets of charge in a controlled manner. These packets of charge can represent discrete-time samples of an analog signal. They can be moved at a controlled rate from an input terminal to an output terminal. The signal appearing at the output terminal is a time-delayed replica of the input signals. The delay which can be realized depends on the number of samples of the input that exist in memory between the input and the output terminals, and the rate at which these samples are moved from input to output. The number of samples that can be stored between the input and the output terminal depends on the basic design of the device; however,

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the rate at which the samples are moved depends on the rate of the clock pulses which is under the control of the user. It is, therefore, possible for the user to control the resulting delay in any manner he so desires within the limits of the particular device and those imposed by the sampling theorem.

For those who watch old movies either at the pizza parlor or on TV, one might envision a long line of firemen passing buckets of water from the cistern to the fire. Such a line is usually referred to as a bucket brigade. It is not surprising that one commonly used charge-transfer device is called a Bucket Brigade Device, BBD.

The bucket-brigade concept of sampling and delaying an analog signal has been of interest for many decades. It was not until the development of MOS integrated circuits that a practical method of implementation became available.

The basic structure of the MOS bucket brigade is shown in Figure 1. This device in its integrated form was invented by Sangster (Ref. 1, 2) at Phillips in 1968. There was much interest in this device since it offered a first glimpse of a practical way of implementing an analog delay. However, the initial device had many shortcomings, with the major one being very poor transfer efficiency, i.e., transfer inefficiency is a measure of the amount of charge left behind at each transfer. As a result, the device was limited to but a few stages and to low-frequency applications since the amount of charge left behind depended in these early devices on the amount of time allotted for the transfer.

The first major advance made in improving the transfer efficiency was also made by Sangster (Ref. 3, 4) and his co-workers at Phillips. It came from the introduction of an isolation or tetrode structure with a d-c biased gate separating each clocked element from its neighbor, as in Figure 2. This tetrode structure in effect reduced the Miller capacitance between the output and the input of each individual stage similar to the function performed by the tetrode grid in a tube. The performance was greatly improved, but still limited to audio frequencies and to a relatively small number of transfers. At about this time the charge-coupled device (CCD) was invented at Bell Telephone Laboratories (Ref. 5). CCD showed the promise of making possible charge-transfer devices without the shortcomings which appeared inherent in the bucket-brigade device. In short, CCD looked to have all the potential advantages that were at first associated with the bucket brigade. The CCD appeared to be a very simple structure requiring only simple processing. However, despite the theoretical improvement, the simple structure with the simple process produced devices not much better in performance than the bucket-brigade devices on which there was supposed to be improvement. It

took five years and many millions of dollars to develop the understanding and technology to the point which allowed these advantages to be truly realized.

It was at this point in the development of charge-transfer devices generally that a closer look was taken by Reticon at the underlying BBD structure, the technology and the processing techniques. Self-aligned structures would reduce parasitic capacitance and improve efficiency. A decrease in substrate resistivity would help to reduce the sensitivity to voltage and to clock wave shape. It would also reduce the conductivity modulation of the region under the transfer gate, which should improve transfer efficiency. However, junction capacitance effects would be adversely affected. It was then determined that, using modern technology, one could selectively control resistivity and its effects by ion implantation--conductivity could be high where wished, and low where wished. The bucket brigade could have the advantages of a high-resistivity basic substrate for minimum junction capacitance but without its deleterious effects on modulation, etc. The desired low-resistivity areas could be selectively controlled. Further, the ion implantation could be used to control thresholds so that N-channel devices became eminently feasible, with all the consequent advantages of higher speed, better transfer efficiency, etc., which follow from the higher mobility of the carriers. Figure 3 shows a comparison of transfer efficiency for both N and P channel audio delay. The superiority of the N channel device is obvious.

APPLICATIONS OF BBD TO ELECTRONIC MUSIC

Having developed an efficient, high performance, externally controlled analog delay device such as the Reticon SAD-1024, the question arises how can it be applied to the electronic enhancement of sound. Many desirable, as well as interesting, acoustical effects may be synthesized with an analog delay device. A partial list of these effects includes enhancement and control of reverberation, generation of chorus, flanging, vibrato, as well as the reduction or cancellation of undesirable effects such as wow and flutter introduced by some tape machines. At this point let us discuss a few of these applications. We will begin by discussing chorus and phasing effects.

CHORUS (MULTIPLE VOICE) AND PHASING (FLANGING) EFFECTS

If a solo voice or instrument is joined by the same sound delayed by approximately one to five milliseconds, the resultant is a very popular "spacey" sound. The phenomenon sounds as if there were two voices or instruments present. This is particularly true if the pitch of one is varied slightly (i.e., the two are not exact replicas). If the resultant signal is again delayed and added as before, the

effect is that of four voices, etc., until delay becomes so large as to cause blurring. Delay can thus be used to enhance or modify the apparent size of a group of musicians (or speakers, etc.,). The SAD-1024 is readily adapted to such use. Figure 4a shows two delay elements in a stable, nonfeedback arrangement of this application. Additional delay elements can be added, as desired, without loss of stability.

Chorus produced by simple delay alone (without modifying pitch or other characteristics) is likely to sound thin and lifeless because each reproduction is an exact counterpart of the previous signal. The effect of slightly different sources can be produced by varying the clock rates by a small amount as in vibrato (and as indicated in Figure 4a). The amount of variation is much less than with vibrato, because the pitch change should not be evident. What is wanted is just enough difference between the direct and delayed signal to make them appear to come from separate sources, i.e., in "chorus."

When the desired effect is that of several different voices added together, it is possible to vary the clock rate slightly but in a random rather than regular manner. Such a clock rate might be derived from noise passed through a narrow-band filter. The output frequency is changed as in vibrato, but the randomness simulates the slight differences in sources, rather than conventional vibrato with one or more deterministic sources. The exact combination desired is subject to artistic interpretation; no rules can be given.

Use of the circuit of Figure 5, but with appropriately small delays, might be thought equivalent to Figure 4a; however, the effect then would be reverberation more like that of "singing in the shower." Sounds build and decay over a period of time; there is not the abrupt start and stop of the ensemble, but rather an exponential rise and decay of sound. The circuit of Figure 4b thus is more realistic for chorus, but either circuit can give subtle or noticeable effects to the extent desired.

Flanging is a sound effect somewhat similar to chorus. It can be obtained with a circuit similar to that of Figure 4b. Variables at the control of the operator are the balance between the direct and delayed signal and the amount of delay. Delay is controlled very simply by control of the clock frequency.

Delay is given by

$$T_D = N/2_{fc}$$

where N = number of delay elements
f_c = sampling clock frequency

For example, for N = 1024, a range of f_c from 50 KHz to 500 KHz gives a range of delay, T_D, from 10 msec to 1 msec. Qualitatively, the frequency response is comb-like with peaks spaced 100 Hz at 10-msec delay and spaced 1000 Hz at 1-msec delay.

VIBRATO AND OTHER EFFECTS

Vibrato is defined as a slight pitch variation at a cyclic rate, usually of the order of 5 to 10 Hz, such as that produced by the rapid oscillatory movement of the fingering hand of a violinist. It is customarily used to add a richness to the sound. The result of vibrato is the combinations of sounds from various paths to give a slight chorusing effect. Such pitch variations can be synthesized by changing the delay element's clock rate in a slow cyclical manner (see Figure 6). Changing the clock rate alternately increases and decreases the delay through the device and hence the pitch in a fashion analogous to the Doppler effect. If the clock rate changes slowly, we can consider the transit time of the delay element to be constant for any particular instant of the input waveform. Delay is thus given by

$$T_D = N/2f_c \text{ seconds}$$

where T_D = the transit time (delay) through the device
N = the number of storage sites in the bucket brigade
f_c = the sampling clock frequency

The factor 2 in the expression for T_D appears because the signal sample moves from cell to cell on each clock transition (i.e., two cells per complete clock cycle).

Now suppose f_c is varied cyclically by a small amount such that

$$f_c = f_{co}(1+k\cos\omega_v t)$$

where f_{co} is the average sampling frequency
$\omega_v = 2\pi f_v$ is the vibrato angular frequency
k is the per unit peak frequency deviation of the clock frequency

The transit time is then

$$T_D = N/[2f_{co}(1+k\cos\omega_v t)]$$

Usually, $k \ll 1$, and T_D can be approximated by

$$T_D \approx \frac{N}{2f_{co}}(1-k\cos\omega_v t)$$

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This expression demonstrates the fact that when clock frequency is high, delay time is low, and vice versa.

To find the frequency variation, we use the definition that angular frequency is the rate-of-change of phase and note that the phase of the output is delayed relative to that at the input by the product of the input frequency, ω_s, and the transit-time delay, T_D. Thus the output phase, ϕ_{out}, and frequency, ω_{out}, are given by

$$\phi_{out} = \phi_s - \omega_s T_D = \omega_s t - \omega_s T_D$$

$$\omega_{out} = d\phi_{out}/dt = \omega_s\left[1 + \frac{Nk\omega v}{2f_{co}} \sin\omega_v t\right]$$

where ϕ_s is increasing at the angular rate $\omega_s t$ (linear if ω_s is constant as assumed for this discussion), f_{co} is the average clock frequency, as before.

As expected, if the time delay is momentarily decreasing, the output frequency is momentarily increasing and vice versa. The magnitude of the peak frequency change is not great, and is controlled by the magnitude of the change in clock frequency in the factor k.

As an example, let

$N = 1024$ (i.e., 1024 elements of delay)

$f_{co} = 50$ KHz

$k = 0.05$ (i.e., 5% peak change in clock frequency)

$\omega_v = 7 \times (2\pi)$ (i.e., a vibrato rate of 7 Hz)

Then: $\omega_{out}/\omega_s \mid max = f_{out}/f_s \mid max$

$$= 1 + \frac{1024 \times 0.05 \times 2\pi \times 7}{2 \times 50 \times 10^3}$$

$$= 1 + 0.0225$$

That is, the output vibrato peak-to-peak frequency change is seen to be 4.5 percent of a steady-state input frequency. As a comparison, a musical half-step of total change is slightly less than 6 percent.

Chorus and vibrato applications are similar to reverberation applications: high performance of the device is required. Here again the superior performance of N-channel devices is important because of their stability and simplified circuit requirements. It is also desirable that neither the d-c bias

point nor the a-c gain varies with clocking frequency. This is another characteristic of the N-channel devices which makes them superior for high-quality low-cost audio applications.

REVERBERATION

Acoustic reverberation is caused by the build-up of sound in an enclosed space. The build-up occurs because of the addition of sound components from simply-reflected and multiply-reflected pencils or rays of sound returned from internal reflecting surfaces. Similarly, the sound field present when sound from the source is suddenly terminated does not die away immediately but decays in an exponential manner as the reflected sounds diminish by acoustic absorption.

Reverberation can thus be synthesized as in Figure 5. Each delay element represents the time of travel in some possible path from the source S to the observer at O. Feedback adds the effect of multiple-reflection paths. Differing path lengths are represented by differing delays. A single delay element can produce reverberant effects, but would be excessively frequency sensitive with the reverberant sound having distinct flutter. Several different path lengths (delays) are desirable. Attenuation in a path represents its acoustic absorption loss; therefore, the adjustment of loss allows the control of reverberation time.

In an actual room the direct sound is received first, followed by simple reflections, and then by an increasingly complex mix of multiple reflections. Thus an equivalent synthetic reverberator must be equipped to generate and handle a similarly complex combination of signals. Let us first consider the general situation.

Reverberation time is defined as the time (after cessation of the signal at the source) for the sound to decay to one-millionth of its energy level (to a level 60 dB down). Let us consider a simple case with only one closed-loop path active. The relationship is

$$T \text{ (reverberation time)} = 60(t/\alpha) \text{ seconds}$$

where (dB) = the attenuation and t = time delay in seconds for one passage

For example: if t = 100 milliseconds and α = 3 dB, then T = 2 seconds. Notice that shorter reverberation times can be produced by introducing greater attenuation or shorter delay; longer reverberation requires longer path delay or less attenuation or both. Also notice that a 10-millisecond delay corresponds to a room path length of less than 10 feet for one trip; as a result delays longer than 10 msec are usually

used. Round-trip attenuations of less than 3 dB lead to narrow peaks in the comb-like frequency response and thus present more difficulty in maintaining stability; so it is preferable to use a mix of relatively long delays with higher values of attenuation. If short delays are used (e.g., 10 msec), then small values of loop attenuation are required to keep the effect, due to short delay, from dying away rapidly. Stability of gain is most necessary.

If, as may be done, we add the output signals from the various delay elements (see Figure 5) the output power is increased approximately in proportion to the number of paths, N. The result is an overall system gain of 10 log N dB. As a result, increased loss should be introduced in the individual path attenuators, as additional paths are added, if the same total reverberation time is to be maintained.

Feedback around a single delay element gives rise to a comb-filter type of response of amplitude vs. frequency. Schroeder (Ref. 6) has developed methods of reducing the frequency sensitivity of the resulting filter and shows various combinations of filters to achieve reverberation characteristics comparable to that of actual rooms. Schroeder further states that some improvement is obtained by converting a comb-filter type of reverberator to an all-pass type of filter. Details may be found in the listed publications. In essence, the number of paths to be summed, the delays which are selected, and their manner of combination during implementation depend on the particular application and the cost/performance tradeoffs of the system under consideration. Ideally, many parallel delay paths are required to simulate acoustics of a desirably reverberant room; practically, at least four, and preferably more, parallel paths are required if undesirable flutter is to be minimized. Adding all outputs into a single feedback path simulates actual room conditions more closely than a group of parallel paths, each with separate feedback; however, adjustable gain. Individual preference as to feedback path should rule.

The frequency response of the delay device is of particular importance in this reverberation application because (a) long delays are desirable and (b) multiple passages through the device result in amplification of gain variations. The high-frequency loss in gain of a bucket-brigade device tends to be a fixed amount at a fixed fraction of the clock frequency, with the -3 dB point between one-third and one-half the clock frequency. To obtain a long delay calls for the minimum allowable clock frequency and hence the forcing of high-frequency attenuation in the desired pass band. The N-channel SAD-1024 is substantially better than comparable P-channel devices in control of this high-frequency attenuation, since the product of the maximum

delay and the usable bandwidth is in the order of two times that attainable with a P-channel device.

The loop transmission factor in reverberation applications must be nearly unity. The SAD-1024 with its near-unity gain is substantially easier to use than comparable P-channel devices with 8 to 10 dB insertion loss. To achieve effects comparable to room reverberation requires that a large number of modes be present. These modes must be spread over time in the time domain (i.e., spread in frequency in the frequency domain). The mode spread must also take into account the acoustical responses of the ear. That is, low frequencies and high frequencies must die away more gradually than middle frequencies to compensate for the ear's variation in frequency sensitivity at different sound levels. The ultimate requirements are that the ear be unable to distinguish different rates of decay (i.e., of the different modes), and that the number of modes be great enough that objectionable flutter is avoided.

CONCLUSION

The availability of high performance analog delay devices has resulted in a whole new array of products that electronically enhance sound.

The performance necessary to make these products possible could only be realized by applying modern technology to the design of the analog delay. Only the N-channel BBD can offer the high transfer efficiency, high sampling frequency, wide bandwidth and large dynamic range at a cost-effective price necessary to realize high performance audio components.

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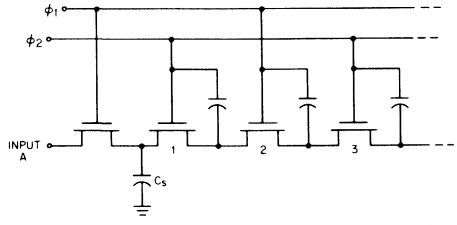


Figure 1. Basic Bucket-Brigade Structure

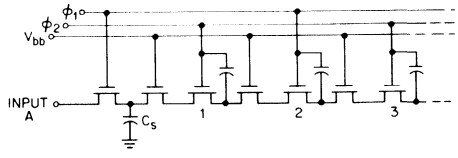


Figure 2. Improved Bucket-Brigade Structure with Tetrode Isolation

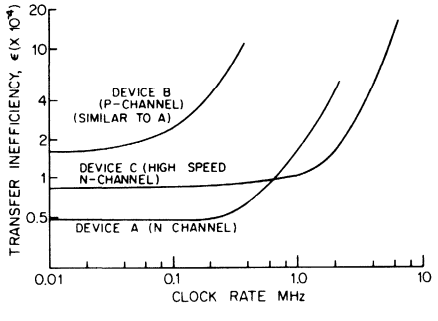


Figure 3. Transfer Inefficiency vs. Sample Rate for Two Commercial Audio Devices and One High-Speed Device

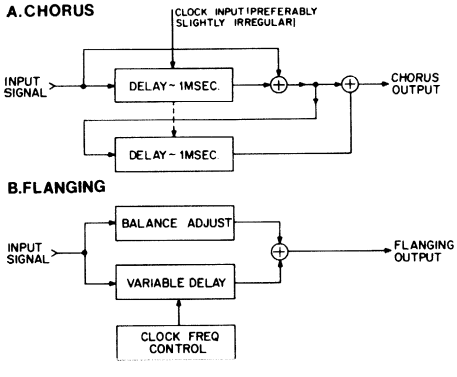


Figure 4. Circuits for Production of Chorus and Flanging Effects

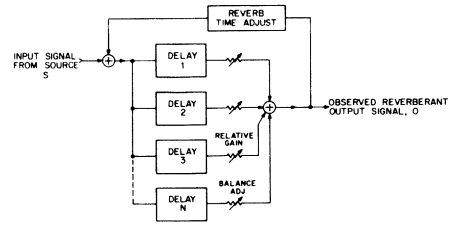


Figure 5. Production of Synthetic Reverberation

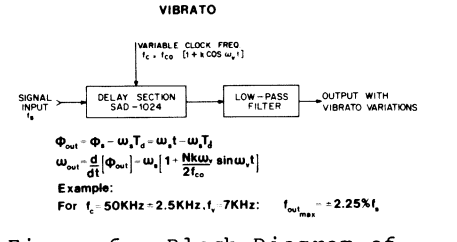


Figure 6. Block Diagram of Circuit for Producing Vibrato Effects

A TAPPED ANALOG DELAY FOR SAMPLED DATA SIGNAL PROCESSING

Abstract

A new dimension in analog signal processing is now available to the engineer. A 32-tap sampled-analog delay line offers a cost-effective way of implementing linear phase filters, performing correlation, realizing adaptive phase equalizers and many other functions heretofore accomplished by digital techniques.

1. INTRODUCTION

The Tapped Analog Delay (TAD) is a 32-stage charge-transfer device. Each stage is tapped and these taps are brought to the outside through buffer amplifiers. Each buffer amplifier output appears as a source follower, thus permitting variable loading of the taps in order to create various tap-weight functions. The TAD-32 permits the storage of analog signals which can be non-destructively sensed at successive delay times. The taps are spaced one sample time apart along the delay. An additional special feed-forward output tap is provided so that devices may be connected in cascade without causing a discontinuity in the spacing of the taps from one device to the next. With this arrangement, timing integrity is maintained. The ability to cascade devices permits the user to build processors (such as transversal filters) with more than 32 taps.

2. GENERAL DESCRIPTION

The Tapped Analog Delay is a new silicon integrated circuit which provides the design engineer with a whole new bag of tricks. The delay line characteristic of this device can be modeled by the series of sample-and-hold (S/H) circuits shown in Figure 1. Two-phase sampling is shown where the even-numbered S/H's sample when the ϕ_2 switches are closed and the odd-numbered S/H's sample when the ϕ_1 switches are closed. As a result, each input sample is sequentially moved from a given S/H to the adjacent S/H on each clock transition. For

a particular input sample to reach the output of the fifth S/H requires five clock transitions, and for that same sample to reach the eleventh S/H requires six more clock transitions. In CTD terminology, each S/H is called a stage, and a given sample of information remains in a stage for one sample time. If desired, any stage could be non-destructively read out to obtain a delayed replica of the input signal. In sampled-data systems the delay between the taps is inversely proportional to the sampling frequency, thus providing flexibility and stability not available with a continuous-time system, as will become more evident later when filters are discussed. The sampled-data system has the flexibility of a digital system without the complexity, cost or power consumption.

The equivalent circuit of the TAD-32 is shown in Figure 2. Samples are set up on the initial storage node during the period while the ϕ_1 clock waveform is at its high (positive) level. When ϕ_1 drops, the sample value is frozen and the simultaneous rise of ϕ_2 permits exchange of charge with the tap-1 node, similarly for other nodes. The sample values thus first appear at the various nodes when ϕ_2 rises. When ϕ_2 falls and ϕ_1 rises, the charge state is transferred to the second node for each tap, thus maintaining the output value for both halves of the clock period. The resulting output is designated full-wave (or full-period) output. Further, there is one sample time delay between the samples as they appear at successive output taps. The last node supplies a feed-forward tap at the proper time to provide the set-up signal for another, series-connected TAD-32, so that multiple-section processors with more than 32 taps can be implemented. Clocking of the second device must be synchronous with the first, i.e., $\phi_{1A}=\phi_{1B}$.

The device is capable of sampling at rates from 100 Hz to more than 5 MHz. This capability permits the translation in frequency of a given filter characteristic over a range of more than four orders of magnitude simply by varying the clock rate. A two-phase clock is required to drive the device with complementary square waves with amplitude in the range of 12 to 15 volts. These are positive square waves, as sketched in Figure 2, thus providing a positive output with reference to ground at each tap. The output from each tap is a full-wave or boxcar output, as discussed above; no additional filtering is necessary before summing the desired weights. The summing amplifiers can combine the summing and filtering functions.

Figure 3 shows the performance of a TAD-32 operated as a low-pass filter. The impulse response of this filter is very nearly a Hamming window; therefore, one would expect the peak side lobes to be suppressed by -43 dB relative to the center lobe or passband. The experimental results of Figure 3 for a sample rate of 120 KHz indicate that -41 dB was achieved.

The width of the main lobe at -20 dB is 12 KHz, which compares favorably with theory. It is apparent that band edge rates in excess of 80 dB/octave are possible. Furthermore, this characteristic can be realized over a 50 dB range of input signal as is apparent from the spectrum analyzer photograph of Figure 3.

This picture shows the spectral response or filter characteristic obtained for two inputs differing by 40 dB. The background response is for an input level 20 dB below the maximum level, thus from this picture one must conclude that nearly 60 dB of dynamic range is possible while still realizing a -40 dB stopband-to-passband ratio. From this we must agree that the performance attainable from the TAD-32 exceeds by far most other approaches. We will now discuss the realization of this performance in useful filter responses.

3. THE TAD AS A TRANSVERSAL FILTER

The Tapped Analog Delay is the basic building block of the transversal filter. The transversal filter represents the most effective application of charge transfer devices to sampled-data signal processing. The signals that appear at each tap of the TAD are weighted and summed by the technique shown in Figure 4. The ability to externally control the weight on each tap allows the user to design a wide variety of filter functions all based on the same basic component, and by switching in different tap-weight functions it becomes possible to program in a predetermined way a desired set of filters. For example, a time-multiplexed filter bank could be realized using one TAD and multiplexing the taps to several tap-weight functions, each derived with resistors.

The output of a transversal filter or finite impulse response (FIR) filter depends on a finite number of past values of the input. This type of realization does not require feedback and as a result coefficient accuracy, lack of signal-to-noise, or non-linearities are much less critical than in recursive or infinite impulse response (IIR) filters, where feedback is employed. An FIR with a non-recursive implementation has all its poles at the origin in the Z-plane and, therefore, is always stable. And finally, one of the most advantageous properties of a finite impulse response filter is that it may be designed to have an ideal linear phase characteristic.

With the introduction of data communication systems, phase characteristics of filters have become as important as their amplitude characteristics. In general, when a signal is passed through a filter, which has a non-linear phase characteristic, the signal waveform undergoes an asymmetrical distortion, which severely degrades a digital communication system. The transversal filter offers two approaches to

remedy the ills of phase distortion. First of all, if only finite impulse response filters with linear phase are employed, there is no phase distortion. On the other hand, should phase distortion already be present, the transversal filter offers one of the most straightforward, cost-effective ways of performing phase equalization. Equalizers can be designed that will flatten the amplitude response while correcting the phase distortion. Special filters synthesized for communication systems can substantially improve the overall system performance. The use of a low-pass filter with linear phase to prevent anti-aliasing in data acquisition systems is a typical example of an application which can best be accomplished with a transversal filter. The alternative to the transversal filter is an analog filter with its characteristic limitations of stability and accuracy.

The transversal filter does not excel in just one or two of these areas. It offers the best obtainable performance in every one of the aforementioned areas. To some, this may sound overzealous; however, those who have had the opportunity to actually implement a transversal filter will fully appreciate the performance potential now within easy reach.

4. PRINCIPLES OF TRANSVERSAL FILTERING

4.1 THE TAD AS A BI-POLAR CORRELATOR

Probably one of the simplest functions that can be performed with a TAD is that of bi-polar correlation. Let us first consider the correlation of two valued (bi-phase) sequences as depicted in Figure 5. As shown in the figure, each tap has a switch in series with it. Sequence A is used as a program word for the switches, i.e., a "1" in the sequence represents a closed switch, while a "0" represents an open switch. Sequence B is sampled into the charge transfer delay line. The sample rate must, of course, be selected so that the delay through the line equals the period of the sequence, i.e., the sample rate must equal the data rate in the sequence. The output signal is a measure of similarity between the two sequences and reaches a maximum when two identical sequences are in perfect alignment.

Let us now consider replacing sequence B on an analog signal as shown in Figure 6. Since the analog signal has both positive and negative values, it is desirable to add a second pole to the switch so that, as shown in the figure, each tap may take on either a plus "1" or a minus "1" value depending on the switch position, thus controlling which input of the differential amplifier is selected. Sequence α (n), which is the tap-weight function, is now represented by a p-n sequence, i.e., positive-negative values. As in the previous example, the amplitude of the output is a measure of

similarity between the analog input signal and the p-n sequence represented by the tap-weight function.

Let us now ask how we would mathematically represent the relationship between the input signal X (k) and the output Y (k), where k represents the k^{th} sample time. Let the tap-weight function be represented by α (n) where n is the tap position with n = 0 being the input, n = N-1 being the last tap farthest from the input, and for the case of the two-pole switch shown in Figure 6, α (n) = $\pm$1. The k^{th} output, i.e., the value of the output Y for the k^{th} sample period, corresponds to the values of the input for the period between the (k-n) and the k^{th} sample times. This is merely a statement of what samples of the input exist in the delay line at the time just following the acquisition of the k^{th} sample. The N previous samples are present in the line with the $(k-n)^{th}$ sample residing at the n^{th} tap. Therefore, the signal at any given tap is given by the (k-n) value of the input times the value of the n^{th} tap weight. The output for any given sample time is given by the summation of outputs from all the individual taps, which yields the following expression relating the output, the input, and the tap-weight function:

$$Y(k) = \sum_{n=0}^{N-1} \alpha(n)\, X(k-n) \qquad (1)$$

This expression is referred to as the convolutional summation and can be shown to be the discrete-time or sampled-data equivalent to the convolution integral of linear systems theory.

A further analogy to linear systems theory can be made by identifying the tap-weight function as the impulse response of our sampled-data system. This may be demonstrated by entering a single non-zero sample into the TAD and observing the output. Referring to the mathematical expression for the output, it is apparent that for each value of k an output appears from only one tap, since only a single non-zero sample exists in the line. Therefore, as this single sample is clocked through the line the output will be a sequence representing the tap-weight function, hence the impulse response of the sampled-data system.

So far it has been shown that the tapped analog delay can perform the function of correlation and that its system function is in reality a discrete-time convolution of a sequence representing a repetitive sampling of a continuous-time input signal and a sequence represented by the tap-weight function. This is consistent, since for even functions, correlation and convolution are equivalent.

The tap-weight functions discussed so far have been simple bivalued functions so that an intuitive feel could be developed for the actual processes that were taking place in the system. Although binary sequence and p-n sequence correlators are often employed, their realization by digital hardware becomes prohibitive when increased accuracy is desired, due to the power and size requirements. The Tapped Analog Delay line in a single device allows analog accuracies in excess of seven bits of binary accuracy to be obtained with simple resistive loading of the taps. The capability immediately suggests the realization of an analog correlator with impulse response matched to a given signal; this realization is normally referred to as a matched filter.

4.2 THE TAD AS A MATCHED FILTER

The matched filter is a concept that finds extensive applications in all signal processing, in particular in the area of spread spectrum communications and radar. A filter is said to be matched to a particular desired signal if its impulse response is a time-reversed replica of that signal. We have previously discussed this type of operation when deriving the mathematical expression for the output from the Tapped Analog Delay. The above definition of a matched filter was for the time domain, and since it is a convolutional process, we know that in the frequency domain a multiplication is taking place between the two frequency functions, i.e., the spectrum of the input signal times the spectrum of the tap-weight function. Therefore, one would expect the real value to be a maximum when the two frequency functions are conjugate functions. This then says that the impulse response should be the Fourier Transform of the conjugate spectrum of the frequency function being sought. This is analogous to the familiar property that maximum power transfer occurs for a conjugate matched load.

To further appreciate the matched filter, let us consider the example depicted in Figure 7. The input to the TAD is a linear frequency chirp. As depicted in Part A Figure 7, the chirp starts with a low frequency and ends with a high frequency. Part B shows the successive samples of the chirp which exist in the TAD at the time just following the acquisition of the last sample. We see that the first sample exists in the N^{th} stage of the TAD and the second sample exists in the N-1 stage, etc. It is obvious from the description that in order to match the chirp of the input signal it would require the tap-weight function to be the time reversal of the input function.

Much more could be said about matched filters, their design, and their application, but the concept of matching the time reversed impulse response to obtain an ideal correlation is the important concept to remember.

Another important concept that should be remembered with respect to transversal filters is that the frequency domain representation is the Fourier Transform of the impulse response. This suggests the possibility of realizing a variety of filter responses by simply tailoring a tap-weight function appropriately. This, in fact, is true and leads to the discussion of the realization of what is referred to as finite-impulse response filters.

4.3 THE TAD AS A FINITE IMPULSE RESPONSE FILTER

The next question to be addressed is, what techniques are used to select a tap-weight function that will result in a desired filter characteristic. There are numerous detailed treatments of this subject in the literature. The discussion to be presented here will be heuristic rather than rigorous. The objective is to help the potential user of the TAD-32 develop an insight to the performance of finite impulse response transversal filters.

One excellent way to develop insight into the interaction of tap weights on filter performance is to implement a TAD-32 with a potentiometer for each tap. It is possible to simultaneously observe both the impulse response and the spectral response while varying the tap weights.

Let us begin the discussion of how to select a tap-weight function by examining the responses obtained from several rather simple tap-weight functions. Figure 8 shows three tap-weight functions: a) all taps given the same value, b) an alternating sequence of plus and minus values, each value separated by a zero, and c) an alternating sequence of pairs, each pair separated by a pair of zeros. The tap-weight function shown in Figure 8 is a rectangle of width N/f_s, where N is the number of taps, f_s is the sampling frequency, and $1/f_s$ is the time between taps. A rectangular pulse has a familiar Fourier Transfer as shown in Part D of the figure. As one might have anticipated, this rather simple tap-weight function leaves much to be desired as a filter. This will be rectified in a later section. For the time being, let us try to develop an appreciation for the overall concept before tackling the details.

Let us now look at the alternating sequences of Parts B and C. The dotted lines show the sinusoidal inputs that would most nearly correlate with these tap-weight functions. As one might have anticipated, these latter two tap-weight functions have each produced a band-pass characteristic, however, at different frequencies. These are shown in Parts E and F. The resulting filter responses, however, maintain the sin x/x characteristic obtained from Part A, where all taps had the same value.

Let us assume that Sequence B was obtained from Sequence A by the multiplication of Sequence A by Sequence B, i.e., tap 1_a X tap 1_b, tap 2_a X tap 2_b, etc. Multiplication in the time domain infers convolution of frequency functions. We know that the frequency function for the rectangular window of A is a sin x/x function and we saw that a definite correlation exists for a particular frequency for Sequence B.

A single frequency in the time domain appears as a delta function at that frequency in the frequency domain, hence a convolution between a delta function at f_0 and any other function is a shifted version of that function centered at f_0. We should, therefore, not be surprised that both of the band-pass responses have the same shape as the low pass translated to a higher center frequency.

Let us recall from the above discussion of matched filters that the impulse response of the filter, i.e., the tap-weight function, is the Fourier Transform of the spectral response of the filter. Suppose we wish to design a low-pass filter. Figure 9a shows the desired frequency response. The Fourier Transform is shown in Figure 9b. Since we have only a finite number of taps, it is necessary that we truncate the time function, choosing (N-1)/2 values on each side of zero. Choosing the tap-weight function to be an even function assures that the filter will be linear phase. It is, therefore, necessary for the tap-weight function to be symmetrical around the center tap. The bandwidth of the filter is the reciprocal of the equivalent time separation between the center of the tap-weight function and the first zero crossing of the tap-weight function. It is usually desirable to try to make the impulse duration as long as possible. This infers that the sample rate for a filter should be as near the Nyquist rate, i.e., the maximum information frequency, as is possible and still be able to realize the desired filter shape. For example, if the choice is between using three zero crossings and four zero crossings of the sin x/x to realize the same bandwidth filter, one would realize a longer impulse duration using four zero crossings, thus giving the best ratio of stopband-to-passband rejection, even though the size of the taps between the third and fourth zero crossing are quite small and contribute little to the resulting output. This results because for the same cutoff frequency, it would necessitate different sampling rates; therefore, four zero crossings would have the lower sampling rate, thus a longer impulse duration for the same number of taps. The tap weights for a 31-tap low-pass filter are obtained from the following expression:

$$\alpha(n) = \frac{\operatorname{Sin} \frac{\pi}{A}\left(n - \frac{N-1}{2}\right)}{\frac{\pi}{A}\left(n - \frac{N-1}{2}\right)} \qquad (2)$$

where n is the tap number starting at the tap nearest the input and progressing to the output end
N is the total number of taps being used
A is the number of zero crossings each side of center

Figure 10 shows the resulting frequency response for the unwindowed filter. This is not exactly what we had in mind.

It is apparent that to improve the characteristics of these filters it is necessary to somehow disguise the fact that tap-weight function is finite. The effects of truncation are a result of approximating a function which exists for all time, by a finite number of terms. For example, the Fourier series of a square wave has an infinite number of terms; however, a square wave may be approximated quite closely using only a finite number of these terms. However, when only a finite number of frequency terms are used, oscillations will occur at discontinuities in the time function. The converse is also true, i.e., if only a finite number of time samples are used to approximate a frequency response. This phenomenon leads directly to the discussion of window functions.

The process of terminating a series after a finite number of terms can be thought of as multiplying the finite length impulse response by a finite width window function. In a sense, the window function determines how much of the original impulse response is actually seen, so the term window is quite descriptive. In the case where the series is abruptly terminated without modification of coefficients, the window function is said to be rectangular. The rectangular window function can be considered as a source of the oscillations as demonstrated in the previous example. Since it is necessary to terminate the series with a finite number of terms, the question arises whether there might be a better window function for this purpose. It is possible to gain some insight into this concept by considering again the terminated series to be represented as a product of an infinite length impulse response and a window function. Since multiplication in the time domain corresponds to convolution in the frequency domain, the actual frequency response may be considered as a convolution of the desired frequency response and the frequency response of the window function. It has already been seen that a rectangular window function produces a rather poor filter. There exist numerous other possible window functions that minimize some of the

difficulties encountered with the rectangular function. In order for the spectrum of the window function to have minimal effect on the desired amplitude response when the two functions are convolved, it is necessary that the window spectrum approximate an impulse response. Obviously, an ideal impulse spectrum is impossible since this would require an infinitely long window. In general, the spectrum of a window function consists of a main lobe representing the middle of the spectrum and various side lobes located on either side of the main lobe. It is desired that the window function satisfy the two criteria: that the main lobe should be as narrow as possible, and that the maximum side lobes should be as small as possible relative to the main lobe. It turns out that both of these criteria cannot be simultaneously optimized, so that most usable window functions represent a compromise between these two factors. A window function in which minimization of side lobe width is the primary objective would tend to have a sharper cutoff but might suffer from some oscillations in the passband and significant ripple in the stopband.

Conversely, a window function in which minimization of the side lobe level is the primary objective would tend to have a smooth amplitude response and very low ripple in the stopband. The sharpness of the cutoff might not be as great. Table 1 shows a comparison of some of the more generally used window functions. For work with the TAD-32, it has been found that the Hamming window function is one of the easiest to apply and gives very good results. If we now return to our previous example, where we chose the sin x/x impulse response, and we multiply that impulse response by a Hamming window.

The result spectral response is shown in Figure 10 as the windowed filter response. A marked improvement in the side lobe rejection is quite apparent as well as a very steep fall-off. Cut-off edges in the neighborhood of 80-100 dB per octave are not uncommon with a 32-tap transversal filter. This same characteristic may be translated to a higher frequency by multiplying the terms by the appropriate sequence, as shown in the previous example of Figure 8, thus forming band-pass filters at whatever frequency one wishes to center the filter. Furthermore, since the characteristics are all dependent on the clock or the sample rate, it is possible to shift characteristics, shifting either the band edge or the center frequency of a bandpass merely by changing the sampling frequency. This provides flexibility not normally available from a filter.

5. CONCLUSION

The TAD-32 offers a means by which the theory that has been developed for digital filters and digital processing can be implemented directly in analog form without the need for

analog-to-digital conversion. Thus, the advantages of digital signal processing can be combined with the speed and simplicity of analog circuitry.

It is especially well suited for realization of a wide variety of filters including low-pass, band-pass, matched, linear phase, as well as programmable and time-multiplexed filters. In addition to its technical advantages, it offers a cost-effective way of implementing these functions.

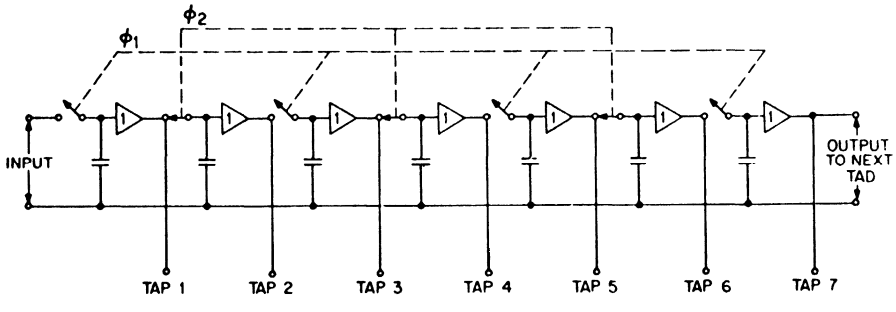


Figure 1. A Tapped Analog Delay Line Made with Sample and Holds

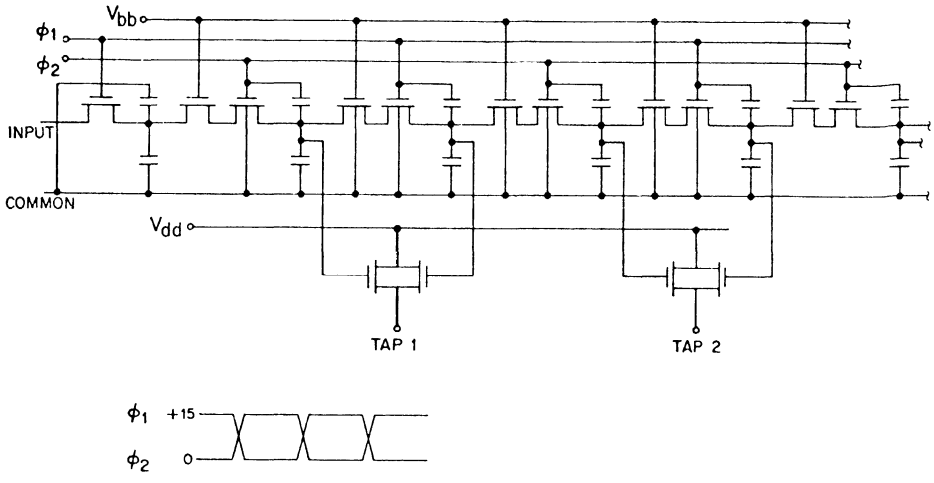


Figure 2. A Tapped Analog Delay Line Made Using Metal-Oxide-Silicon Integrated Circuit Technology

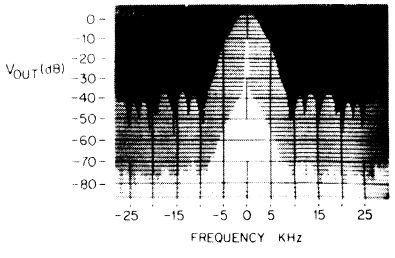


Figure 3. Photo of Spectrum Analyser Output with Hamming Window

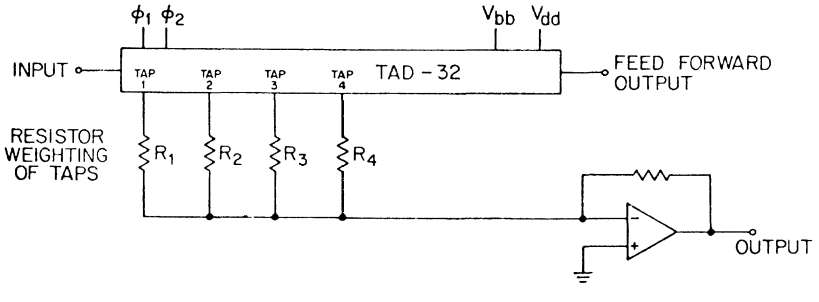


Figure 4. Schematic Representation Showing Resistor Loading of Taps for the Realization of a Desired Filter Function

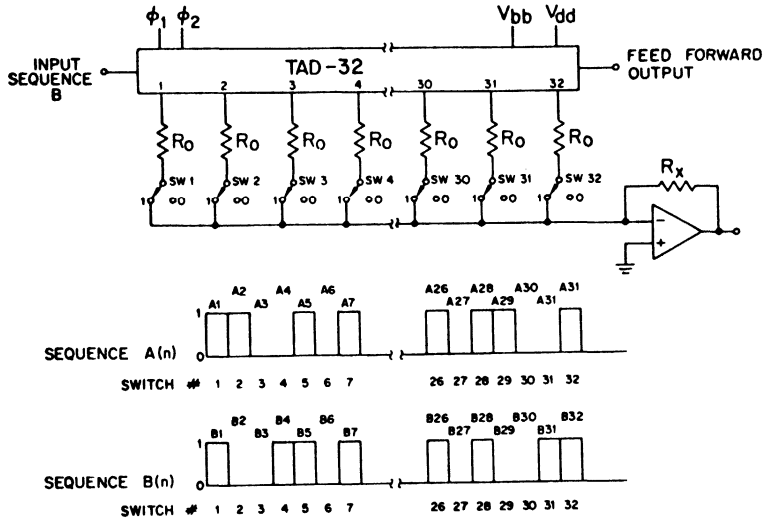


Figure 5. Schematic Showing Tapped Analog Delay Performing Binary Correlation

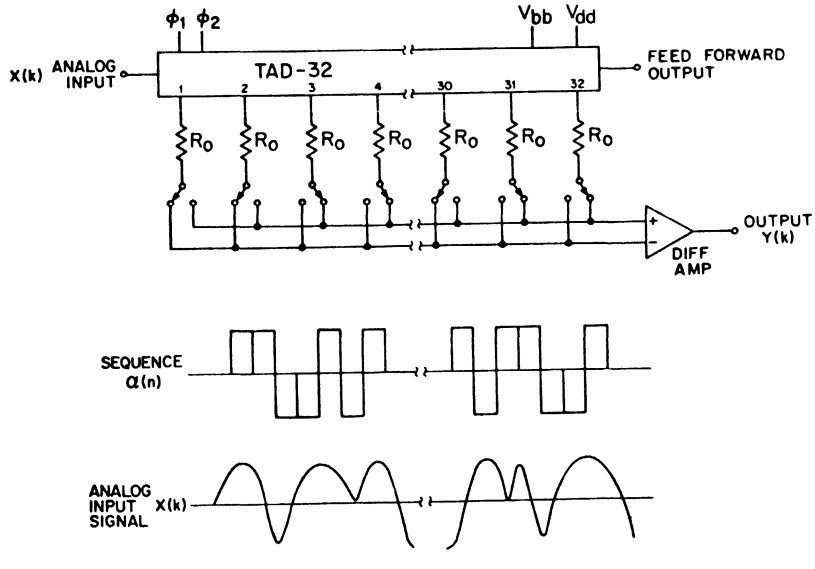


Figure 6. Schematic Showing the Tapped Analog Delay as a Bivalued Analog Correlator

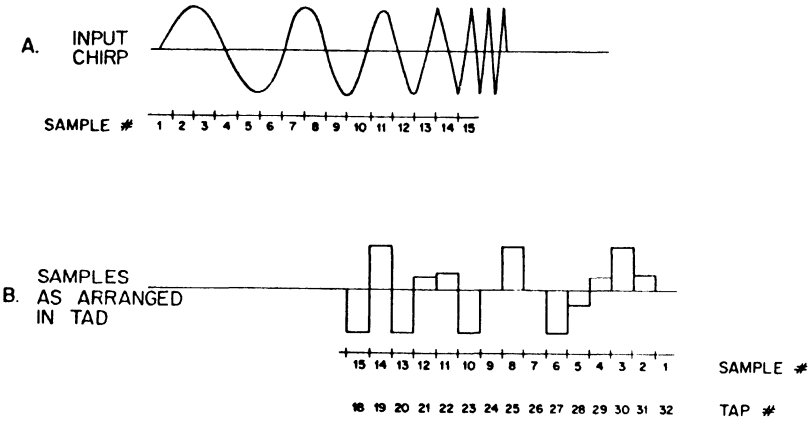


Figure 7. Arrangement of Samples of Input Chirp Along the Length of a Tapped Analog Delay

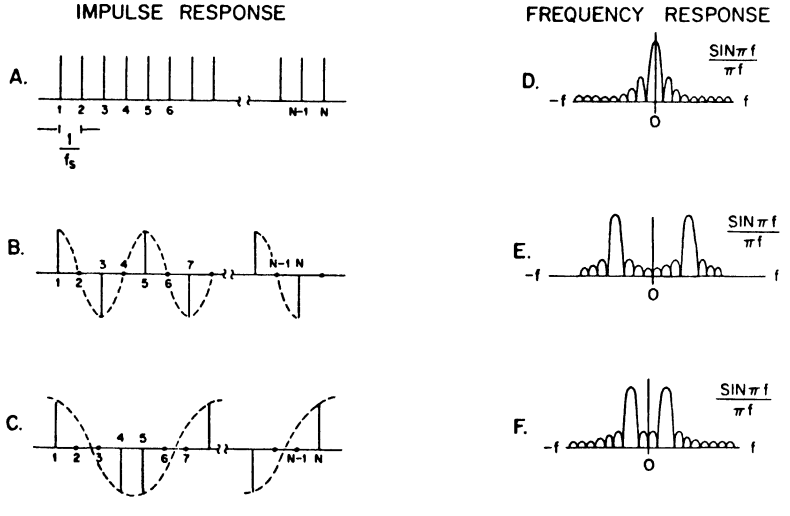


Figure 8. Three Simple Impulse Responses and the Resulting Frequency Response Produced by Each

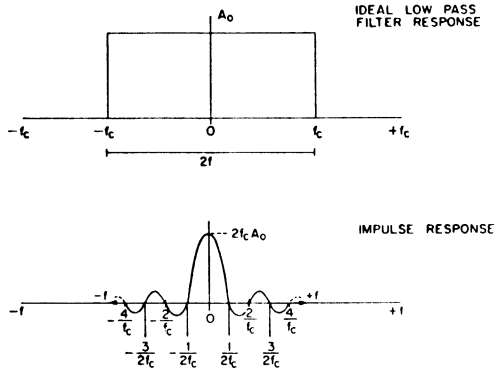


Figure 9. Impulse Response for an Ideal Low-pass Filter

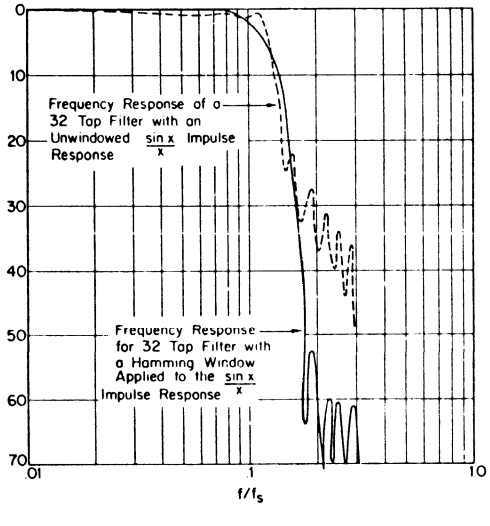
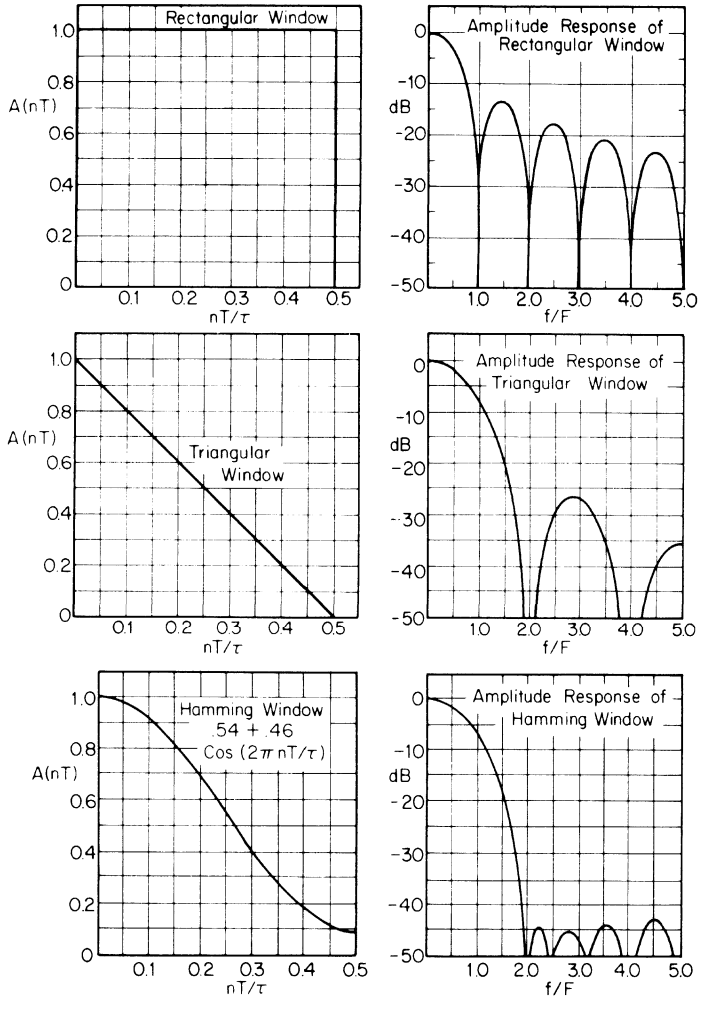


Figure 10. Comparison of Windowed and Unwindowed Filter Response



τ = Width of window function
T = Time between samples
n = Sample number (all window functions are even with only half shown)
F = 1/τ

Table I. Comparison of Commonly Used Window Functions

BUCKET-BRIGADE DEVICES

CIRCA 1977

ABSTRACT

The bucket brigade was a development of the late 60s, at which time it was quite extensively studied. The major shortcoming was found to be inadequate transfer efficiency, thus relegating its usage only to audio applications. Before the problem could be solved, charge-coupled devices appeared which showed promise of improved transfer efficiency, higher clocking frequencies and higher density; therefore, most of the work switched from bucket-brigade devices to charge-coupled devices. New processes were developed in order to make charge-coupled devices that could truly realize their predicted potential; however, with these new processes and with charge-coupled devices working fairly well, the question was never asked what improvement could be realized in a BBD if both modern technology and modern understanding were applied.

This paper will described the modern bucket-brigade device. Transfer efficiencies of 0.9998 have been obtained at 5 MHz sampling rates while at lower rates an efficiency of 0.99995 is not uncommon. Bucket-brigade technology is such as to permit simple adaptation to tapped delay-line configurations, with easy and precise control of tap weights. This capability is of great importance, as it permits BBDs to transcend simple delay applications and enter the very broad field of discrete-time filtering. Interfaces with other MOS devices on the same chip likewise are easy to implement. The modern BBD thus leads to the efficient realization of simple delays, tapped delays, and programmable tapped delays--both real time and erasable--as well as to correlators and transversal filters. In many cases a BBD offers a simpler and more effective solution than would a corresponding CCD or the much more complex fully digital system.

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INTRODUCTION

The basic structure of the bucket brigade is shown in Figure 1. This device in its integrated form was invented by Sangster (ref. 1, 2) at Phillips in 1968. There was much interest in this device, since it offered a first glimpse of a practical way of implementing an analog delay. However, the initial device had many shortcomings, with the major one being very poor transfer efficiency. Potential variations during the charge-transfer period introduced excessive channel-length and barrier-height modulation and consequent transfer inefficiency. As a result, the device was limited to few stages and to low-frequency applications.

The first major advance made in improving the transfer efficiency was also made by Sangster (ref. 3, 4) and his co-workers at Phillips. It came from the introduction of an isolation or tetrode structure with a d-c biased gate separating each clock element from its neighbor, as in Figure 2. The performance was greatly improved, but still limited to audio frequencies and to a relatively small number of transfers. About this time the charge-coupled deviced (CCD) was invented at Bell Telephone Laboratories (ref. 5). CCD showed the promise of making possible charge-transfer devices without the shortcomings which appeared inherent in the bucket-brigade device. In a BBD, the charge must be transferred from capacitance to capacitance under the control of the separating MOS transistors. In the switching process, there is an uncertainty or noise in the capacitive charge transfer over the intervening barrier that is proportional to κTC and somewhat analogous to thermal noise in a resistance. κ is Boltzmann's constant, T is absolute temperature, and C is the capacitance being charged. The CCD arrangement did not have discrete capacitances separated by barriers, so this noise source appeared to be absent, and, further, clock-line capacitances to be driven were smaller so that driving problems should be less severe. The CCD in concept was a very simple structure requiring only simple processing. In short, CCD appeared to have all the potential advantages at first associated with the bucket brigade. Nonetheless, performance fell far short of expectations. It took five years and millions of dollars to develop the understanding and technology to the point which allowed these postulated advantages to be truly realized. It was then that a re-examination of bucket-brigade technology was initiated. Devices fabricated using some of the modern techniques and employing a tetrode structure were found to perform reasonably well (ref. 4), but transfer efficiencies were still less than one could wish; furthermore, stability was erratic and the devices were sensitive to clock shapes, particularly the transition edges.

DEVELOPMENT OF THE MODERN BBD

At this point in the development of charge-transfer devices, a closer look was taken at the underlying BBD structure, the technology, and the processing techniques. The basic bucket-brigade structures of Figures 1 and 2 employ idealized transistors and capacitors; the physical realization suffers from parasitic effects. The MOS control gates overlap the junctions which are conveniently represented in the figures as nodal points. Any overlap beyond that required to ensure a continuous channel results in unwanted capacitance, particularly capacitance to the prior node. Each nodal diffusion has (depletion) capacitance to the substrate. These capacitances divert charge and increase the difficulty of efficiently providing the desired transfer-clock waveforms. Further, the depletion capacitance is voltage-dependent and so leads to non-linearities in the transfer characteristic. One method to minimize parasitic capacitance is to use self-aligned structures, that is, a processing method whereby one masking step controls the openings for a channel and also the subsequent formation of a control gate which is automatically self-aligned.

The non-linear depletion capacitance would be minimized by a high substrate resistivity, but uniformly high resistivity would lead to excessive sensitivity to the problems of channel-length (conductivity) modulation; and further, high channel resistance leads to poorer high-frequency performance.

CONSTRUCTION FEATURES

Modern technology permits selective control of resistivity by selective ion implantation. One can thus make resistivity high or low where desired. The bucket brigade could have the advantage of a high-resistivity basic substrate for minimum junction capacitance but without its deleterious effects on conductivity modulation, etc. The desired low-resistivity areas could be selectively controlled, as shown in Figure 3. Further, the ion implantation can be used to control thresholds so that N-channel devices become eminently feasible, with all the consequent advantages of higher speed, better transfer efficiency, etc., which follow from the higher mobility of the carriers.

Figure 3a is a plan view of the semiconductor surface showing in linear fashion the organization of the bucket brigade. An equivalent cross-section view is as in Figure 3b. These sketches are exaggerated to show details. The substrate material is p^- material which is then implanted to a p^+ state everywhere except the regions intended to underlie the diffusion between successive clock and tetrode gates (and certain other input and output regions), as shown. The tetrode-gate and clock-gate regions are then masked off and

n^+ material diffused to form the bulk of the signal path. Note that these masked-off regions later receive the polycrystalline silicon control gates in automatic self-alignment with the underlying undiffused channel region; however, the channel region under the gates has been implanted to p^+ concentration so that low-resistivity and positive thresholds are the desired result. In the intervening diffused area, the nodal area of the schematic circuit of Figure 2, there was no ion implant and substrate resistivity is high. The result is that depletion width under the diffusion is relatively large and parasitic capacitance to the substrate small. In a later step, a second-layer poly is applied above the diffused area and connected to the clock gate to the left to form the desired signal-storage capacitance.

Devices have been made using the structures and processes described. Transfer efficiency as high as 0.99997 has been obtained at low sample rates, while values as high as 0.9998 at 5 MHz have been measured.

PERFORMANCE FEATURES

Transfer efficiency is one of the important factors in any charge-transfer device, since it affects the number of transfers possible (and hence the delay) before serious degradation of bandwidth occurs. Quantitatively, it is easier to use the accumulated inefficiency, the product $N\varepsilon$ of the number of transfers N and the inefficiency $\varepsilon(\varepsilon=1 -$ transfer efficiency) in considering the effects. The bucket brigade is a sampled-data system, with the associated restriction that the signal band must be restricted to a range somewhat smaller than the Nyquist limit of $f_c/2$, where f_c is the sample frequency (equal to the clock frequency for the examples given). In this signal band there are two factors causing the high-frequency response (modulation transfer factor) to be less than the corresponding value at low frequencies. The first factor is inherent in the sampled nature, in the fact that the output signal is only a stair-step approximation of the desired analog signal (assuming full-wave output). That is, the output is a sequence of pulses whose successive amplitudes carry samples of the analog values. The representation is good for low frequencies, where many samples per cycle occur, but becomes increasingly poor as the signal frequency rises toward the Nyquist frequency; that is, the signal-frequency component in the stair-step representation is less than the stair-step amplitude by a factor $\sin(\pi f/f_c)/(\pi f/f_c)$. This factor introduces a loss of ~4 dB for $f=f_c/2$.

The second factor is the loss resulting from accumulated transfer inefficiency, which contributes a loss expressible as $R_{dB} = -17.4N\varepsilon\sin^2(\pi f/f_c)$ where R_{dB} is the reduction, expressed in decibels, relative to the response at low

frequencies, f is the signal frequency, and f_c is the sample frequency for the BBD. This expression reaches a maximum value of $17.4N\varepsilon$ dB at $f = f_c/2$. Thus, for 5000 transfers and $\varepsilon=10^{-4}$ (efficiency = 0.9999), the loss is 8.7 dB at $f_c/2$ and 4.35 dB at $f_c/4$. Measured values of transfer inefficiency ε are shown in Figure 4, and its effects on delay-bandwidth product are shown in Figure 5.

The dynamic range is limited at the upper end by signals so large that distortion becomes excessive, and at the lower end by signals too small to be distinguishable from noise. If one ignores all effects from overlap and depletion capacitances, barriers, etc., the maximum peak-to-peak input swing is $\Delta V=(V_{bb} - V_T)\ C_1/C_s$ where V_{bb} is the tetrode gate voltage, V_T is the threshold voltage (assumed constant at the value of body bias present), and C_1/C_s is the ratio of driving capacitance at an interior node to the initial storage capacitance C_s. Consider Figure 2. When ϕ_2 is at zero, ϕ_1 is at maximum and node 1 charges through transistor 2 and the tetrode transistor to $(V_{bb} - V_T)$. Meanwhile, C_s is charged via the input to some potential which is ΔV below $(V_{bb} - V_T)$. When ϕ_1 falls and ϕ_2 rises, the potential on C_s rises by the amount ΔV to $V_{bb} - V_T$ at the expense of the potential at node 1, which falls from $\phi_2 + V_{bb} - V_T$ by an amount $\Delta V\ (C_s/C_1)$. At the next clock transition, the potential at node 1 instantaneously falls back by the magnitude of ϕ_2 to a value $\Delta V(C_s/C_1)$ below its initial terminal value of $V_{bb} - V_T$, and then rises again to $V_{bb} - V_T$ at the expense of node 2. But the minimum potential cannot be less than the substrate potential (assumed zero), so that within the above constraints ΔV max $\leq (V_{bb} - V_T)\ (C_1/C_2)$. Parasitic capacitances and other effects in general act to reduce the maximum ΔV (ref. 6).

Noise generated in the bucket brigade limits low-level signals. Ref. 7 shows the variance per stage in the number of charges transferred at each transfer is proportional to κTC, as stated earlier, with the result that the noise spectral density has two principal factors. The first factor is proportional to κTC times the number of stages and inversely proportional to clock frequency, meaning that noise increases directly with the number of stages and decreases as clock frequency increases. This latter effect is important as it degrades performance at low clock frequencies. Qualitatively, the κTC noise is spread over a very broad frequency range, as is thermal noise, and hence folds about each harmonic of the clock frequency. As clock frequency is reduced, there are more sections of the spectrum folded down into the useful band lying between 0 and $f_c/2$. The second factor is a frequency variable nominally proportional to $\sin^2 \pi f/f_c$ but substantially reduced by transfer inefficiency at the upper end. Figure 6 taken from ref. 7 illustrates this latter effect. $M\varepsilon$ is the accumulated transfer inefficiency. Note that the curves are normalized to show

degradation of transfer efficiency. Futhermore, it is possible to cancel clocking transients because coupling from ϕ_1 through C_a cancels that from ϕ_2 through C'_a, etc. In Figure 9, the relative tap weight is given by

$$w = \frac{C_a - C_b}{C_a + C_b}$$

It is evident that the weight, w, may be controlled over the range +1 (when $C_b = 0$) to -1 (when $C_a = 0$). One thus realizes simplicity of signal extraction, without having to bother with coordination with clocks multiplexed on the same lines as the signals. An example of such design is shown in Figure 10. These are but a few of the unique advantages of the bucket brigade which, with suitable modern technology, make it a device quite adequate for a large number of signal-processing applications.

WHY USE BUCKET-BRIGADE DEVICES?

It is well known that charge-transfer devices are very suitable for analog signal processing. However, most designers immediately conclude that using charge-coupled devices is the only way to do the job. To the question: "Why not use charge-coupled?", the answer is itself a question: "Why not use the device most suited to the task? Why restrict the technology regardless of its suitability?" Bucket-brigade devices have a distinct range of applicability, with many favorable factors such as those discussed:

1. With proper design, transfer efficiency is so high that it need not be considered for many applications.

2. Processing is by standard MOS processing, with high yield and compatibility with other MOS devices, so that flip-flops, clock drivers, shift registers, output buffers, etc., may be designed onto the same chip.

3. One or many taps are easily and precisely implemented, with simple output circuitry.

4. Clocking and other interface requirements are simple and non-critical. There are no tricky multiphase clocks with requirements on precise control of rise and fall times--a simple two-phase complementary square wave clock is all that is required. CMOS clock generators usually are adequate.

5. Output circuitry is equally simple, allowing one to do either capacitive non-destructive sampling of the bucket such as in a tapped delay line (Figure 9), or to use source-followers which are directly (non-destructively)

driven by the buckets and which in turn act as current sources to the outside world. The output circuitry on-chip often dominates the real estate so that packing density of the delay elements themselves becomes of secondary importance.

6. The bucket brigade is capable of sampling to 5 MHz or more. This situation is compatible with peripheral circuitry, which usually is capable of operating in the same frequency range.

SUMMARY

In summary, then, bucket-brigade devices should be used for audio and other low-frequency applications, in some video-delay applications, and in signal processing generally, where the bucket brigade is best suited. It is exceedingly flexible and non-critical in delay applications. With modern technology, it exhibits high transfer efficiency, moderate speed, and simplified interface requirements. It allows one to make transversal filters using split-electrode structures; however, the split electrodes are strictly sensing structures and are not part of the clocking circuit, nor do the structures suffer from overlap capacitance as is typical in CCD split-electrode structures. The sense electrodes are separate from (and balanced to) the clocking electrode structure. Futhermore, in a transversal filter, a processing gain is available because of the summed signals from multiple taps; thus, the device is not as sensitive to noise as would be a simple long delay used, for instance, in audio or video applications.

CCD is needed when extremely long delays are desired, such as an 8000-stage audio delay line where wide dynamic range is also desired. Properly designed CCDs have higher transfer efficiency and a noise limit that does not increase as rapidly as in a BBD when the number of stages is increased. CCDs also should be used when sampling rates significantly in excess of 10 MHz are desirable, or when packing density is of prime importance, and where the penalty of extra complexity is justifiable.

Operation at elevated temperatures limits storage lifetimes, and hence forces a practical limit to the amount of delay possible, or alternatively, to the number of taps possible. Further, in most signal processing applications such as correlators or transversal filters, one finds a limitation imposed by the time required to do the calculation and the number of points in the calculation. Therefore, a time-complexity compromise must be made. For instance, at 1 MHz sample rate, it would take 32ms to compute a 32-point calculation, and 64ms for a 64-point calculation. A compromise must be made between the total number of taps in the device and the speed of the computation. It has been

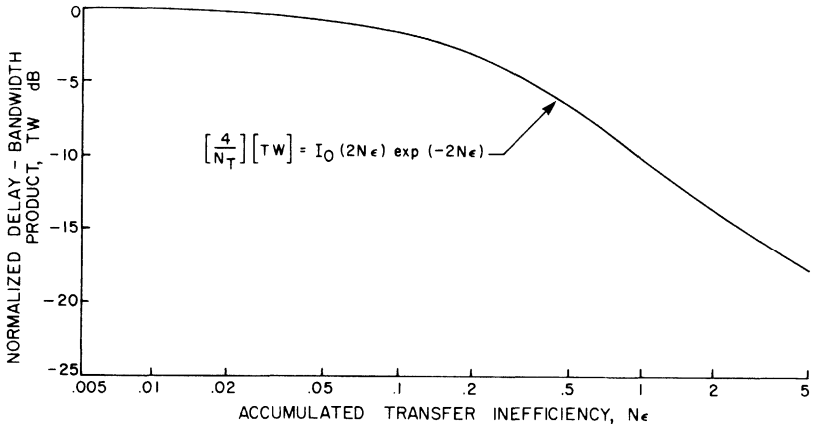


Figure 4. Transfer inefficiency vs. sample rate for two commercial audio devices and one high-speed device.

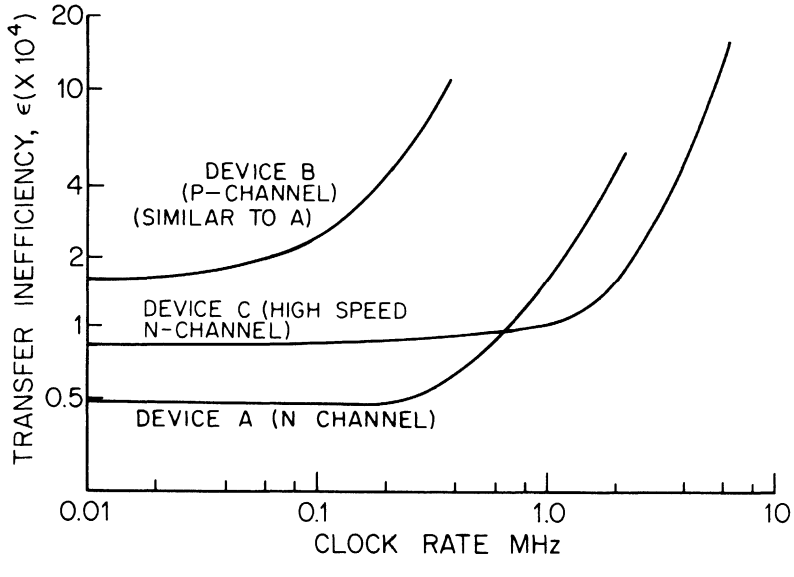


Figure 5. Normalized delay-bandwidth product vs. accumulated transfer inefficiency NE.

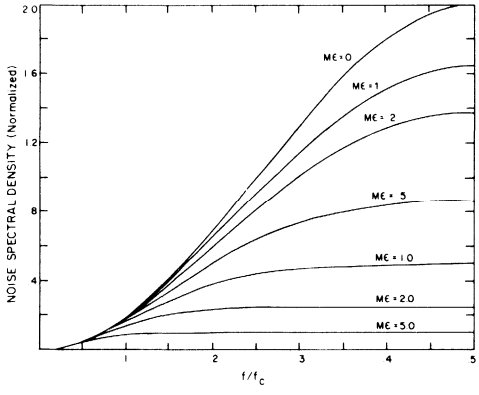


Figure 6. Normalized noise power spectral density as a function of normalized frequency. Imperfect charge transfer severely attenuates the high frequency noise components.

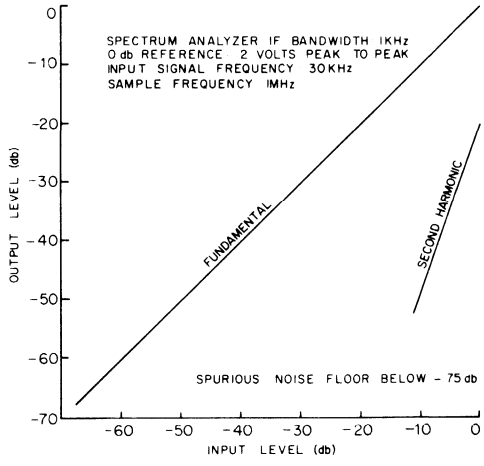
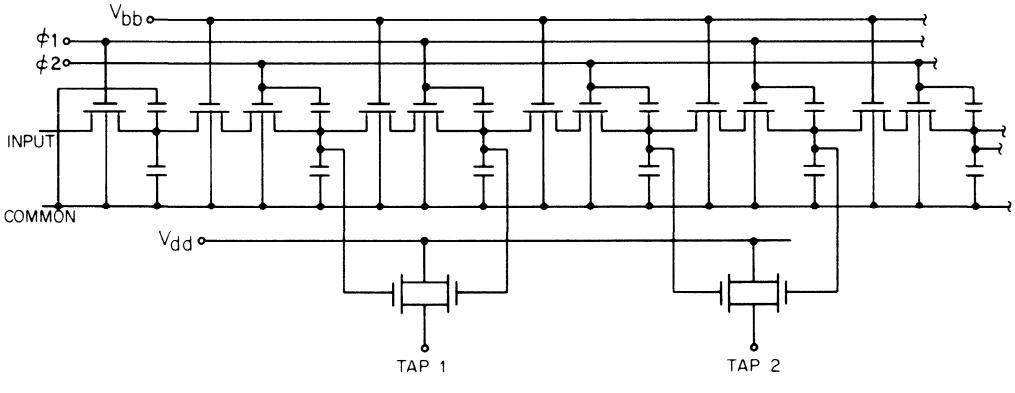


Figure 7. Dynamic range and linearity for tetrode BBD.



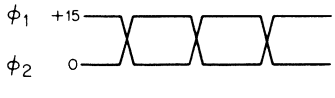


Figure 8. Equivalent schematic circuit for tapped BBD.

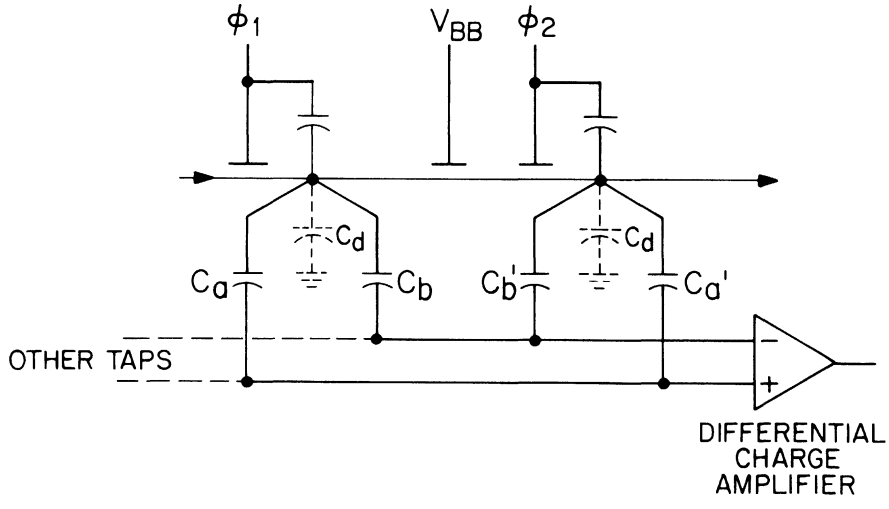


Figure 9. Capacitive divider taps for BBD.

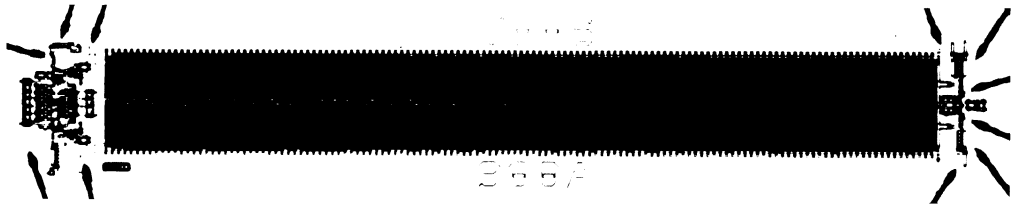


Figure 10. R5171--64 Stage Split Electrode Filter.

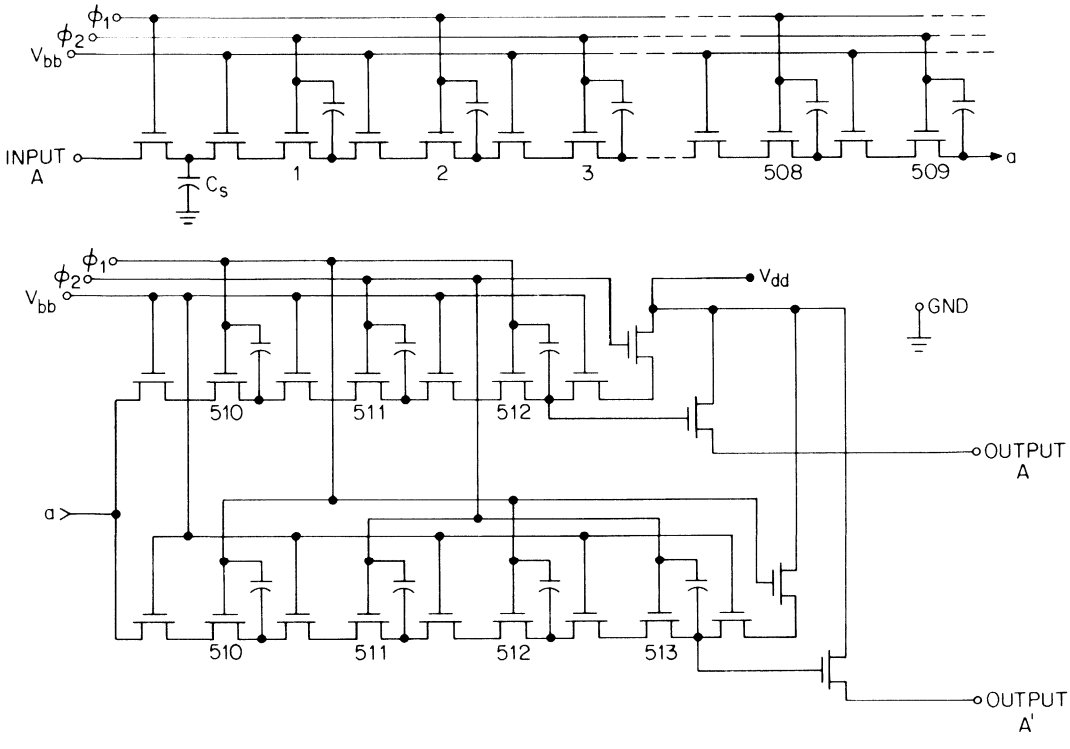


Figure 11. Equivalent circuit diagram for an audio-frequency BBD, the SAD-1024.

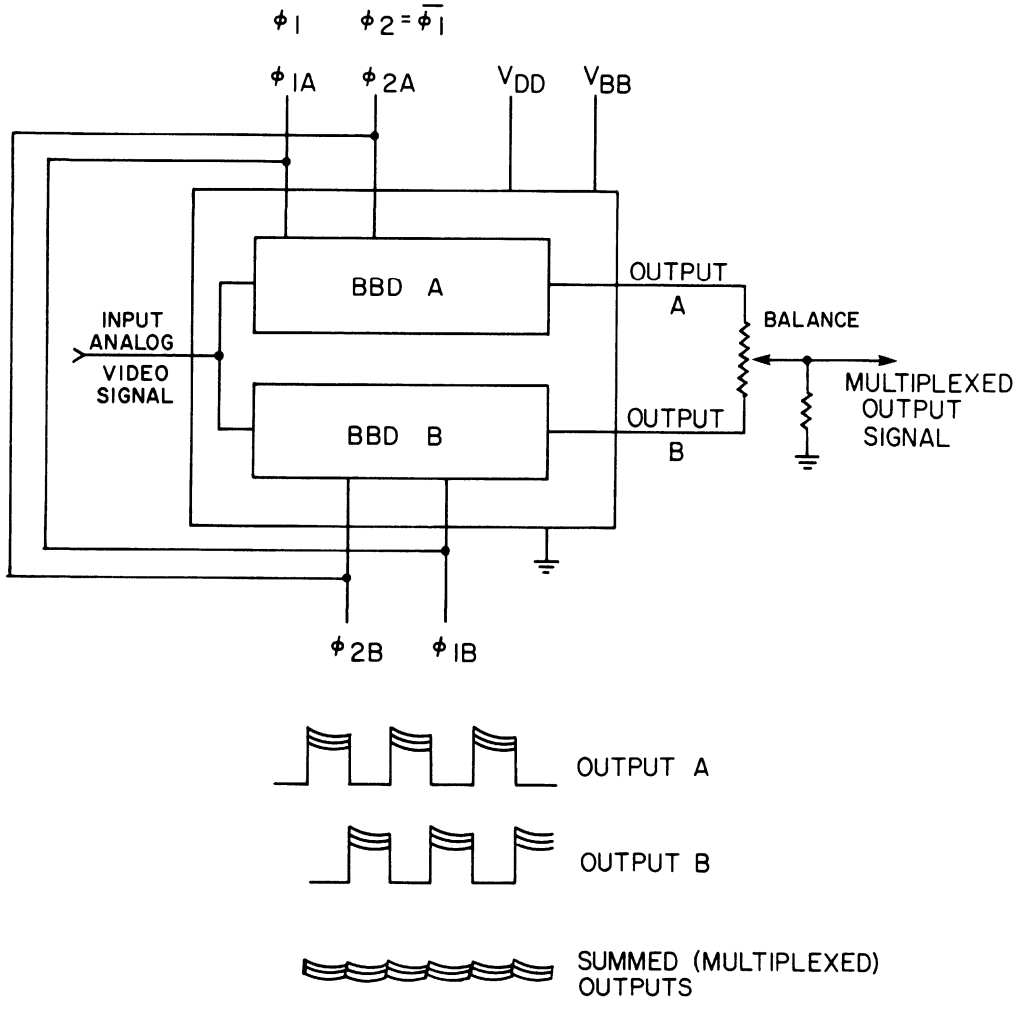


Figure 12. Method of multiplexing delay lines to obtain wide-band high-frequency operation R5103.

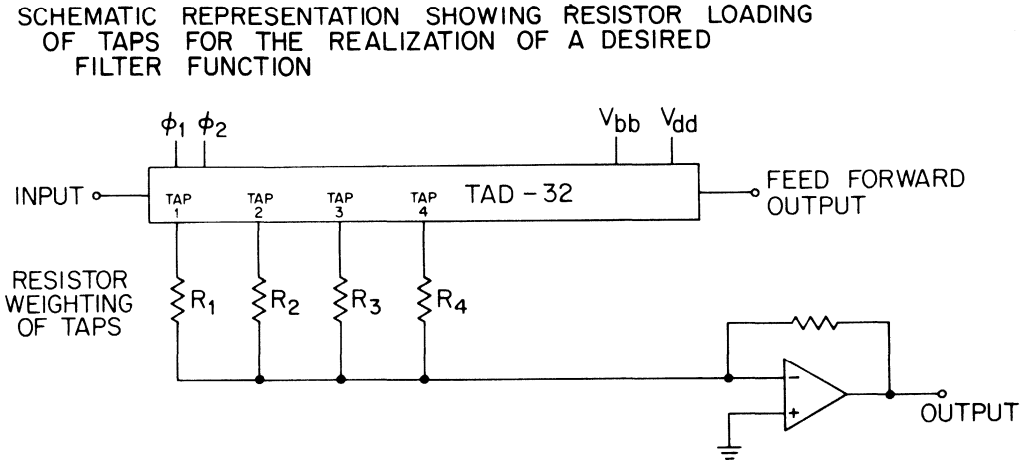


Figure 13. The TAD-32A, a Tapped Analog Delay device.

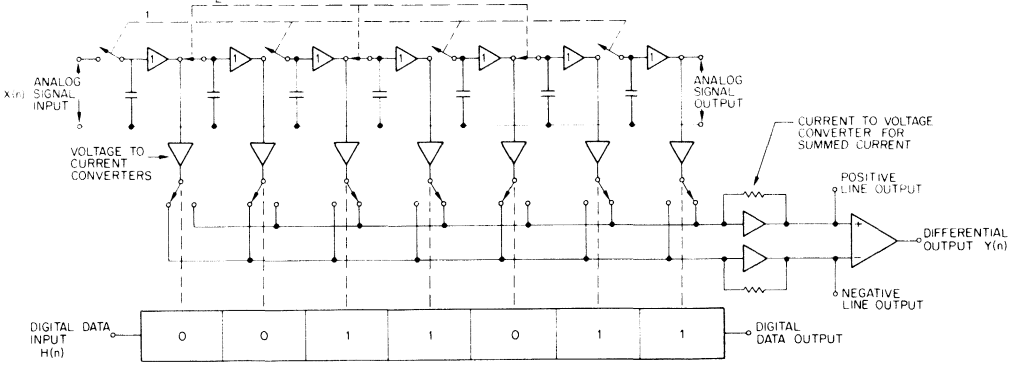


Figure 14. An example of a BBD Binary-Analog Correlator R5401/BAC32.

RETICON Corporation is a subsidiary of EG&G, Inc., Wellesley, Massachusetts.

SERIAL OPERATION OF CLOCKED ANALOG DELAY LINES TO OBTAIN LONG DELAY

Several manufacturers are marketing bucket-brigade clocked analog delay lines for use at audio frequencies. One of these, the SAD-1024 (manufactured by Reticon Corporation), is a new device with substantial improvement over previous devices. It is an N-channel MOS device. It operates with supply, clock, and signal voltages positive with respect to the substrate material, whereas others are P-channel devices which operate with negative voltages. The polarity of supply voltages is incidental to, and a result of, the manufacturing process; voltage polarity is itself not of importance otherwise. More important is the generally improved performance and simplicity of use which applies to N-channel devices and to the design of the SAD-1024. Advantages are:

Only a single power supply is needed (input bias is derived from V_{DD}); the P-channel devices require three or four separate supply levels.

A unity-gain configuration is possible which permits direct cascading of stages without intermediate amplifiers.

Frequency response follows more nearly the limits of an ideal sample-and-hold device; i.e., transfer inefficiency effects are substantially reduced.

Gain and bias are relatively constant as clock frequency varies.

An analog sampled-data device lies in the region between linear and digital devices in its field of application and methods of use. Data is handled on an analog basis, but in discrete time, controlled (typically) by an external clock. Successful application, which is simple and easy, does call for attention to the particular characteristics of a sampled-data device. Generally, the device (with filtered output) behaves as a linear analog delay element, with delay directly controlled by the clock frequency. Internally,

however, signals are handled in packets or samples, at fixed intervals, much as in a digital system, but levels remain variable, as in an analog system.

In simple terms the input signal is sampled at discrete, fixed times, as determined by an external clock, and thereafter all internal handling is applied to these fixed samples. The sample amplitude remains fixed between samples, and clock signals appear as part of the mix. Simple, effective application thus takes into account the sampled nature of the signals.

INTERSTAGE COUPLING

For serial operation, one stage must be coupled to the next, with the proper application of bias voltage. Figure 1 shows the effective circuit diagram of one section of the SAD-1024 bucket-brigade delay line. Input must be applied and stabilized while the ϕ_1 clock is high, to connect the input to the initial storage capacitor C_S; a "don't care" interval occurs during the following half-period of the clock. Output (from unprimed outputs) likewise is valid during the period ϕ_1 is high. Furthermore, on the SAD-1024, the active-period output is typically slightly more positive than the desired next-stage input, so that, for serial operation, the unity-gain configuration permits virtually direct connection of one output to the next input, as in Figure 2. The preferred connection is shown at (a), where the tap on the load resistor controls the exact bias level to the optimum value for the next input stage. Output from one section (during its active-period) is automatically very nearly equal to but slightly more positive than the desired level for the next input, so very little voltage appears across the capacitor. At (b) and (c) are shown simplified alternates to suit various situations. At (b) a common bias voltage may be used for all stages, but the bias source must have low internal impedance to avoid coupling between stages and differences between devices may give rise to non-optimum bias for some if no adjustment is possible. The purpose of the negative source in (b) is to demand more current from the source followers and so reduce their output DC level. The circuit at (c) avoids bias-voltage supplies altogether, but gain is slightly less than unity because the bias-determined value of the load impedance is too low--approximately 1700 ohms instead of the approximate 2500-ohm value desired for unity gain. An adjustable resistor as in (c) but connected to a bias source as in (b) is also useful, as bias may then be optimized.

OUTPUT COUPLING

Once bias values have been set, no readjustment normally is required. Only at the very high clock frequencies of 1/2 MHz and above does optimum bias change significantly, and even there it changes only a few percent. Incorrect bias causes

non-symmetrical peak clipping under maximum or overload conditions. For lesser amplitudes, bias is noncritical.

A circuit for use at the last-stage output, or where capacitor (AC) coupling is desired is shown in Figure 2(d). This circuit fills out the normal half-clock-period output pulses by interleaving output B' with output B. Output B' has been delayed beyond B by one-half clock period as sketched at (d). At (e) is an alternate circuit where the variable resistors permit adjustment to exact balance between the two outputs. Other circuits can be devised; those given are practical suggestions. At (d) and (e), the diodes prevent reduction of the signal level by disconnecting the low-state (nonactive) output. An output capacitive coupling circuit, coupling directly from (b) or (c) or the like and followed by a low-pass filter, automatically suffers a 6 dB loss because the signal exists only on the more positive halves of the pulses, hence (d) or (e) is usually preferable as an output circuit.

PERFORMANCE

Overall frequency response for eight series-connect SAD-1024 sections (four devices) is shown in Figure 3 for various clock frequencies. Each section contributes only one-eighth the total; thus, for one section, bandwidth is greater than the Nyquist frequency ($f_{clock}/2$). It is also to be observed that the overall bandwidth tends to be a fixed proportion of the clock frequency, as expected for such devices. The curves apply to transmission of the sampled data; each normal output filtering of the stairstep signal applies a $(\sin \pi f/c)/(\pi f/c)$ factor where f is the signal frequency and fc is the clock frequency. This factor is unity at f = 0 and causes 3.9 dB attenuation at $f = f_c/2$. It arises because of the elimination of the harmonics of the signal which are present in a square-edged stairstep signal, leaving only the fundamental-frequency component. The factor applies only once to the entire chain. Filtering between individual stages is to be avoided, because the factor would then apply once for each filter. A single filter at the output should have rapid attenuation for frequencies beyond $f_c/2$, so as to eliminate aliasing and residual clock-frequency components.

Once set up and operating as outlined above, the SAD-1024 behaves as a simple analog delay, with delay independent of input frequency, but readily variable by control of the clock frequency. Such delay components have many applications in acoustics and in signal processing generally.

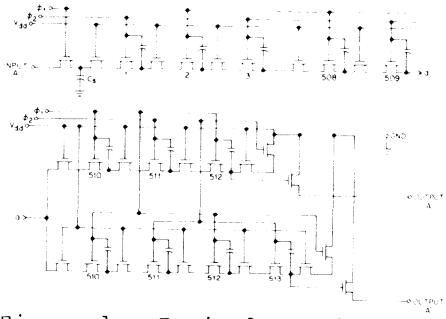


Figure 1. Equivalent Circuit Diagram for One Section SAD-1024

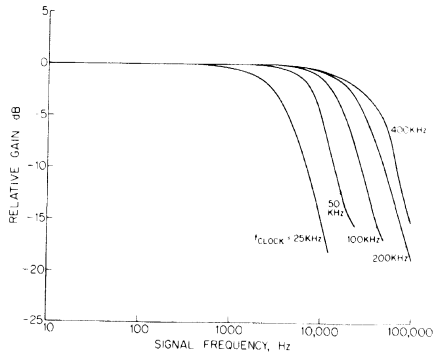


Figure 3. Relative Frequency Response for Eight Sections (Four Devices) of SAD-1024 Devices in Series

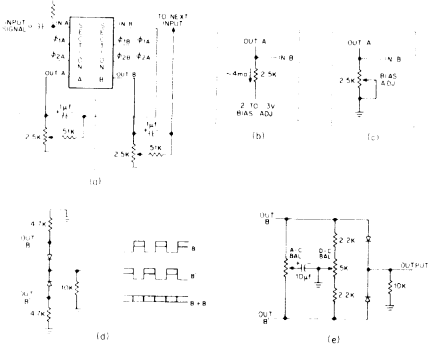


Figure 2. Interstage and Output Coupling Circuits for the SAD-1024

USE OF ANALOG DELAY LINES FOR AUDIO SPEED CHANGE WITHOUT PITCH CHANGE

The development of sampled analog (discrete time) delay devices such as Reticon's SAD-1024 permits an economical and simple means of speeding or slowing recordings of speech, etc., without the pitch change that normally follows. [1-4] The technique for increasing the speed of a recording, for example, consists of:

(1) Physically increasing the playback speed of the recording.

(2) Feeding the output from the recording through a delay system where transit-time delay linearly increases with elapsed time (over a short time span).

(3) Chopping out small sections of the recording by reverting abruptly from the increased value of delay to the original low value and then again causing the delay to increase as before.

These features are both necessary and sufficient, because:

(a) The actual output must occur in real time; therefore, an actual speeded output cannot be obtained unless the total message input is speeded to give an actual decrease in total time duration.

(b) Delay cannot be indefinitely extended; further, if delay were extended over a time significant compared to the message length, there could then be no decrease in total elapsed time, unless accompanied by loss of significant parts of the message. As a result, it is possible only to increase delay for a short time interval and then discard an insignificantly short piece of the message.

(c) The messages typically have adequate redundancy; that is, pitch is maintained longer than is necessary for

articulation. As a result, short sections may be discarded. Pitch recognition and intelligibility still remain. Distortion is introduced, of course, but typical speech may be speeded by a factor of up to two and still remain intelligible.

To slow a recording, the inverse operation must be done:

(1) Playback the recording at reduced speed to obtain the correct time frame.

(2) Restore pitch components to their former values by delaying the signal by a decreasing amount (for short time periods).

(3) Repeat data to fill the gaps that would normally occur when jumping from short delay to long delay preparatory to a new decrease in delay.

The Reticon SAD-1024 is nearly ideal for performing the variable-delay function:

It has enough storage to be useful.

It is simple and reliable in operation.

It has a minimum of unwanted side effects which plague other units.

It has low distortion, a bias level that is constant as clock frequency changes, and a large bandwidth-time delay product; and it requires only a single power supply and very low power. It is simply connected for zero-dB transmission loss.

The delay through the SAD-1024 is a function only of the clock frequency. The delay can be found from the implicit expression:

$$N = 2\int_{t_o}^{t_o + T} f_c dt$$

where

N = the number of storage sites in the delay device (1024 for the SAD-1024)

f_c = the instantaneous clock frequency, which is varying with time

t_o = the reference time a packet of information enters the delay device

T = the transit-time delay

For fixed delay, f_c is constant, independent of time, and $T = N/2f_c$. The factor $2f_c$ arises because the packet moves two cells or sites for each full clock period.

In the present case, we wish T to be increasing or decreasing with time in a linear fashion. The required variation for clock frequency, f_c, is then, for f_c decreasing and T increasing:

$$f_c = \frac{K_1}{t + t_a}$$

and for f_c increasing and T decreasing:

$$f_c = \frac{K_2}{t_b - t}$$

K_1, K_2, and t_b are constants which determine the shape of the time variaton of f_c.

To shorten playback, the recording is speeded up and delay progressively increased so as to reduce pitch to compensate. The delay is then given by:

$$T = K_3 (t_o + t_a)$$

where

$$K_3 = \exp (N/2K_1)-1$$

To lengthen playback, the recording is slowed and delay decreased so as to increase pitch to compensate.

$$T = K_4 (t_b - t_o)$$

where

$$K_4 = 1 - \exp (- \frac{N}{2K_2})$$

In either case, the transit-time delay is a linear function of the entry time of a packet, t_o; a linear increase for the speeded case, and a linear decrease for the slowed case.

A block diagram showing a possible implementation of pitch compensation for changed playback speed is shown in Figure 1. The variation of clock frequency with time is shown for decreased pitch (compensating for speedup); for increased pitch the waveforms are essentially inverted.

At each abrupt change in clock frequency, the electronic switches are reversed to connect the appropriate delay line to the output. While one line is operating in the variable-delay mode to give linearly changing delay, the other is in the flyback and set-up mode. The clock waveshape must be controlled long enough in advance of the switching of the line to active status to permit filling the line with correctly spaced samples; when the switch connects the output to that line, the output then shows a constant effective speed change to compensate for the recorder speed change.

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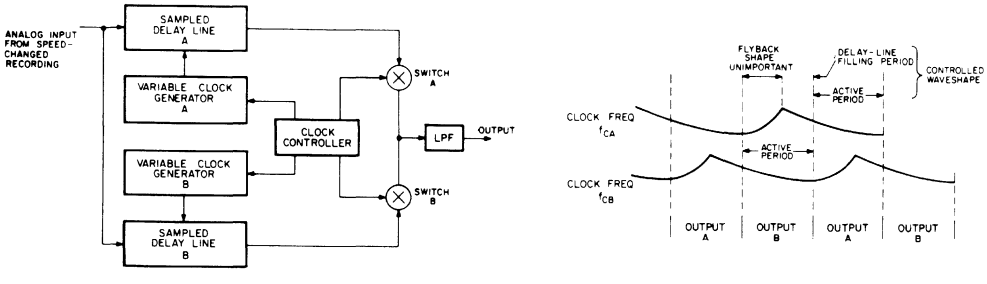

Figure 1. Simplified Implementation for Obtaining Audio Speed Change Without Pitch Change, With Waveforms of Required Clock Accuracy.

CHARGE TRANSFER DEVICES FOR SAMPLED-DATA PROCESSING

I. INTRODUCTION

Charge transfer devices (CTDs) make possible a new type of signal processing, simultaneously offering the characteristics of digital as well as conventional analog approaches. This type of processing is related to digital processing because the data are sampled and therefore are under the control of a master clock, resulting in the same advantages of temperature stability and flexibility of data handling which characterize digital systems. As the amplitude of the sampled data is retained in analog form, considerable reductions can be made in circuit complexity.

Recently, important advances have been made in digital signal processing. As digital signal processing theory relies mostly on the discrete time nature of the signal and not on the quantization of the signal amplitude, direct use can be made of digital signal processing techniques in designing systems using CTD technology. Thus, advantages of low cost, small size, reduced complexity, and low power consumption can be realized.

In this paper, a family of charge transfer devices is discussed. The common feature of this family is the capability to perform discrete-time signal processing. Basically, each device sums of the products of delayed samples of one signal either with samples of another signal or with a weighting function. This operation can be expressed as the discrete-time convolution which is the basic of signal processing. Complex operations such as correlation or filtering can now be done in real time at sample rates up to 10 MHz.

The common features of the devices are presented first--the delay, multiplication and addition features. A universal signal processing device could be built using these basic building blocks, performing any conceivable operation between two signals--either analog or digital--either real time

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programmable or fixed. However, at the present state of the art, the construction of a universal LSI signal processing device would require giving up speed and power and increasing the complexity of the device. For this reason, we have chosen to create several devices which are application oriented, and which bring out the best features for particular applications. The class may be subdivided to distinguish among devices which perform convolution of a sampled-data analog signal with any of the following:

(1) A fixed binary signal.
(2) A fixed analog signal.
(3) A variable binary sequence.
(4) A second sampled-data analog signal.

Another feature of the various devices is that each is programmable one way or another. A weighting function may be entered any of the following ways:

(1) Programming of binary or analog weights by setting a potentiometer.
(2) Real time programming of binary weights by entering a binary pattern into a digital shift register.
(3) Real time programming of an analog weighting function or entering an analog signal into a second analog shift register.
(4) Mask programming of a weighting function.

The following Reticon devices meet several of the above characteristics:

(1) Tapped Analog Delay
(2) Binary Analog Correlator
(3) Analog Analog Correlator
(4) 64-Stage Transversal Filter

The function of these devices and their applications are presented in Sections III and IV.

II. COMMON FEATURES OF THE CTD SIGNAL PROCESSING FAMILY

Why do the CTD devices give us such a powerful technique for discrete-time analog signal processing? After all, their basic capability is merely the ability to delay signal samples, to multiply, and to sum. The explanation is as follows:

The basic equation in discrete time signal processing is the convolutional summation (see Reference 1)

$$Y(k) = \sum_{n=0}^{N-1} H(n)\, X(k-n) \qquad \text{(Equation 1)}$$

where Y(k) is an output sample at the clock period k resulting from the summation of N products of weighting elements H(n) and of delayed samples of an input signal X(k). The convolution concept is appreciated if one realizes that the convolution of two signals in the time domain is the same as the multiplication of the Fourier Transform of both signals X(f) and H(f) in the frequency domain.

$$\underbrace{H(n) * X(n)}_{\text{Convolution}} \longleftrightarrow \underbrace{H(f) \cdot X(f)}_{\text{Product}} \qquad \text{(Equation 2)}$$

Those familiar with the Fourier Transform concept will recognize that the right side of Equation 2 describes the filter action where H(f) is a filter characteristic, and X(f) are frequency components of the input signal. Although the spectral filter characteristic H(f) is easily visualized, its counterpart in the time domain H(n) may be less known. The function H(n), however, is the inverse Fourier Transform of H(f) which is equivalent to the impulse response of Equation 1. Thus any desired frequency response may be generated by determining the weighting coefficients H(n) in this manner.

This type of filter is called a transversal or finite impulse response (FIR) filter. In addition to the ease in determining their desired frequency response, there is an additional advantage to transversal filters. The phase characteristic of these filters can be designed to be linear over the entire frequency range of the filter, so that the time waveform of the input signal will not be distorted.

It would be prohibitively complex to attempt to make sophisticated filters the conventional way by using continuous analog devices. Before the availability of discrete-time signal processing devices, sophisticated filters were possible only by complex digital signal processing techniques, requiring A/D and D/A converters and computers capable of performing the Fourier and inverse Fourier Transform.

Transversal filters have a number of applications in addition to simple spectral filtering, such as matched filtering, single sideband modulation (Hilbert Transform), and spectral analysis.

Another wide area of applications may be addresed because convolution Equation 1 represents correlation if the input signal or the weighting function is reversed. Thus, an analog or binary signal may be correlated in sections with a signal pattern stored in the device, enabling the performance of pattern recognition or decoding. Two analog signals may be correlated if a section of one signal is held stationary temporarily until a section of the other signal is correlated with this section; the stationary signal portion is then

replaced with a new signal section, and the correlation process is repeated. Correlation is applicable to the measurement of the degree of similarity of two signals. It is also used to extract signals buried in noise or to measure the delay of two similar signals carried on two different channels.

III. COMPARISON OF THE VARIOUS CTD SIGNAL PROCESSING DEVICES

As was previously mentioned, charge transfer devices can perform signal processing functions quite naturally. Charge transfer device technology is available to create Bucket-Brigade Devices (BBDs) or Charge Coupled Devices (CCDs). Bucket-brigade devices are normally adequate for analog delay lines up to 256 stages; for longer delay lines, CCDs are preferred, because their stage/chip area density is about twice that of the BBDs. Only in the past few years has implementation of discrete-time analog signal processing devices been possible after improvements were made in the area of CTD technology. With present n-channel technology, charge transfer inefficiencies up to 5×10^{-5} are achieved, enabling high signal fidelity to be maintained when the signal passes through the delay stages.

Figure 1 shows the general structure common to all of the devices of the family discussed. The figure is a symbolic representation of Equation 1. Every clock period a new input sample is taken. Input samples are delayed in a CTD, symbolized by delay elements T_d, where T_d is inversely proportional to the clock frequency. During every clock period, each delayed sample is multiplied by a weight H(1), H(2), etc., and the summation of the products appears at the output.

The main difference among the various devices discussed is the form of the weighting function or of the impulse response H(n) (binary or analog) and the way in which the impulse response is entered into the device (by real time entry or by presetting). Also, the multiplication and addition scheme varies from device to device. Figure 2 shows the various schemes that can be used for the convolution of the sampled-data analog signal with any of the following:

(1) A fixed binary signal--switches selecting certain analog samples are set according to the binary sequence.
(2) A fixed analog signal--multipliers a_1, a_2, etc--are set according to a weighting function.
(3) A variable binary sequence--a static shift register controlling the tap switches is loaded with a binary sequence.
(4) A second sampled-data analog signal--the second signal is temporarily stored in another CTD and its analog samples multiply the analog samples of the first signal.

In Figure 3 are those Reticon devices which fulfill the functions described above, as well as the extent to which the devices are programmable.

IV. DESCRIPTION AND APPLICATION OF THE CTD DEVICES

A. The Tapped Analog Delay

The Tapped Analog Delay (TAD-32) consists of a 32-stage CTD in which each stage is tapped to make it accessible at the device pins. The device is extremely versatile because it is left to the designer to choose and to implement a desired weighting function. The weighting function is implemented by choosing resistors corresponding to the weighting function, attaching these to the proper taps, and summing the resulting weighted analog-sample in an op amp. Positive and negative weights may be obtained by using a differential amplifier (see Figure 4).

The Tapped Analog Delay comes closest to the universal general purpose discrete-time processing device. It can have either a fixed or variable weighting function. Using external resistors, switches, and potentiometers, fixed coefficients can be established.

If it is used with an external digital shift register, or another Tapped Analog Delay, or with microprocessor controlled D/A converters, a system can be built to perform real-time signal processing. Thus, applications from filtering and coding to correlation may be realized with this device. Examples for some of the applications are given in References 2, 3, and 4.

Linearity and noise set performance limits for the signal processing devices. Figure 5 shows the typical harmonic distortion for the Tapped Analog Delay as a function of input signal amplitude. Harmonic distortion is defined in this case as the ratio of the secondary harmonic to the fundamental, expressed in dB. The spectral noise is shown in Figure 6 in comparison to the spectral response for a rectangular weighting function (all weighting resistors with the same value). The dynamic range was determined from this curve by calculating the ratio of maximum useable rms signal to the rms noise up to the Nyquist frequency expressed in dB. The relation of harmonic distortion and dynamic range is shown in Figure 7.

B. The Binary Analog Correlator

The Binary Analog Correlator is a 32-stage CTD in which analog samples are either added on a summing line or subtracted, depending on the position of the switches (see Reference 5). The switch position is controlled by the outputs of a digital shift register (see Figure 8). Thus a

binary weighting function may be entered from the outside, making possible the real time correlation of an analog or binary signal and a binary signal.

Figure 9 demonstrates the powerful capability of this device. How can a binary code such as that shown in the upper portion be detected when it is accompanied by a series of many other codes? To do this by hardware with discrete components is a cumbersome project. The task is made easy with the Binary Analog Correlator. The code to be detected is merely shifted into the binary shift register and is correlated against the incoming signal. The nature of correlation is such that when there is maximum agreement between the stored code and the binary signal, the output becomes maximum. If codes are transmitted--as is the case in radar or satellite applications--the discrimination ratio (the ratio of the highest output signal to the next highest) must be very large. In the example of Figure 9a, a code giving a large discrimination ratio is shown. Figure 9b demonstrates that the Binary Analog Correlator can still pick out the code buried in noise.

A typical application is shown in Figure 10. Periodically, a code is transmitted and echos of the signal are received. The time delay at which correlation occurs between the transmitted signal and the received signal provides an indication of the distance of the object from which the signal was reflected. Coding may be used in a multitude of other applications, for example, in the addressing of various telephone receivers, where each station is assigned its own code.

Because there are 32 stages in the Binary Analog Correlator, 2^{32} or more than four trillion codes are possible. The device, therefore, can be used for decoding messages. It also has the capability to change the code key quickly.

Information coding is extensively used in spread spectrum communications, not for security but to overcome the power and noise constraints. In transmitting information, the information bits are spread out over time and frequency by coding each information bit. At the receiving station the spread information is recombined up again by correlation. The process of coding and decoding in a spread spectrum communication system is demonstrated in Figure 11.

The ability of the Binary Analog Correlator to update the binary correlation word in real time also makes this device useful in combination with a microprocessor. Teaming up both devices, each may perform the task for which it is most suited. Correlation definitely comes more naturally to the discrete-time signal processing device. A 32-point correlation is completed in a BAC in 64 clock periods, or in 6.4 μsec; a microprocessor has to perform 2048

multiplications to do the same task, and also requires more memory. The correlation of an analog signal with another digitally coded analog signal may be performed by paralleling several BACs; each BAC processes a different binary weight. For the correlation of two signals, both in an analog form, the Analog Analog Correlator (see below) is best suited.

Figure 12 shows the function of the 32-stage Analog Analog Correlator (AAC) in which two CTDs are used. The device contains 2 thirty-two stage analog delay lines. A different analog signal may be stored in each analog delay line. Each time a new sample is entered, all existing samples stored in the CTD are shifted one stage. At every clock period, the products of the opposing analog signal samples are summed, giving a measure of correlation at that point in time.

A demonstration of the performance of the Analog Analog Correlator is shown in Figure 13. A triangular waveform is correlated (convolved) with a square wave of higher frequency, resulting in the correlation (convolution) of both. In this case, correlation and convolution are the same because both signals are symmetrical functions. For unsymmetrical signals either correlation or convolution may be performed, becaused the second may be entered from either direction.

The AAC enables one to solve a large number of problems which so far can be handled only by complex equipment or with the aid of computers. For example, in medical research it may be used for the correlation of brain waves emanating from different portions of the brain. In ultrasonic imaging applications, it may be used to enhance the object of interest, for example a tumor, by ignoring the uncorrelated signals caused by the surrounding tissue when viewing the object from different viewpoints.

The ability of the AAC not only to correlate but also to convolve permits its use in filters. Its real time programmability enables its use in adaptive filtering. In telephone networks, a change in the transmission line characteristic may be equalized by altering the filter characteristic through an updating of the weighting function in the second CTD.

D. Transversal Filter

In applications which require a large quantity of the same filter, the Transversal Filter is recommended. This filter has a split electrode structure as shown in Figure 14. The weighting function is determined by the size of capacitors which sense the analog signal samples at the CTD taps. The weighting functions are mask-programmed similarly to the methods by which ROMs are programmed. Three types of filters were created by this technique which will cover another wide

area of applications. These are 64-stage filters with a weighting coefficient accuracy of 1/2 percent. A FORTRAN computer program was used to determine the weighting coefficients. The program is capable of synthesizing optimal linear phase filters from an arbitrary frequency response (see References 6 and 7).

Figure 15 shows the frequency response of the filters which were designed for a minimum peak deviation from the desired response, an extremely high rolloff, and an out-of-band rejection of approximately 50 dB. One filter has a low-pass, the others have narrow and broad band-pass characteristics. The high spikes in the curves are caused by the dc response of the spectrum analyzer.

The filters show a rolloff greater than 100 dB/octave which, up to now, can be accomplished only by complex multi-stage circuits when using conventional analog devices. With the peripheral clock circuitry, these filters can be built on a four-square-inch circuit board. The weighting function of the filters is evident by measuring the impulse response (see Figure 16).

The frequency characteristic of the mask-programmed discrete-time filter is not completely committed. The band edges and the bandwidth are functions of the clock frequency. Therefore, the spectral band to be filtered may be varied by adjusting the clock frequency to a filter-dependent multiple of the center frequency. An application taking advantage of this feature is a spectrum analyzer using several narrow band filters (see Figure 17). Each successive filter is clocked by half of the clock frequency of the previous filters, thus covering a spectral range from $f_{cl}/4$ to $f_{cl}/4x2^n$ where f_{cl} is the frequency of the master clock and n is the number of ÷ 2 stages in the counter. Simple filters have to be used ahead of the CTD filters to limit the signal up to the Nyquist frequency in order to avoid aliasing.

It appears that simple filter using the transversal device will find applications in the touch tone system. The large quantity used in this field will certainly justify the cost of mask programming. The strong existing effort in making talking computers using vocoders in this area will also result in a demand for filters having unique frequency responses that can be implemented easily.

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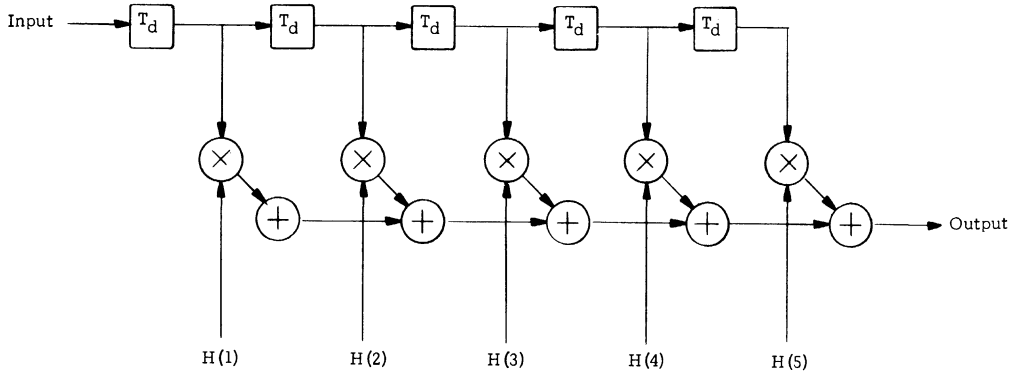
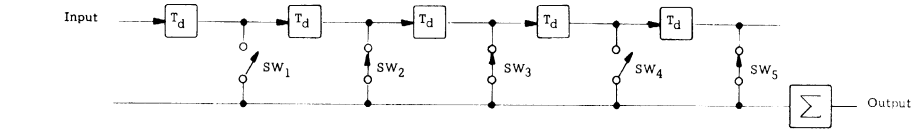
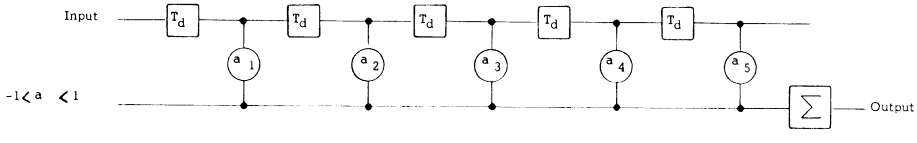


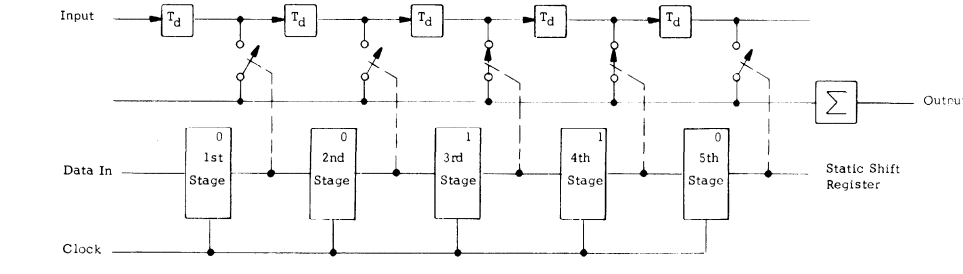
Figure 1. General Symbolic Representation of a Discrete-Time Signal Processing Device



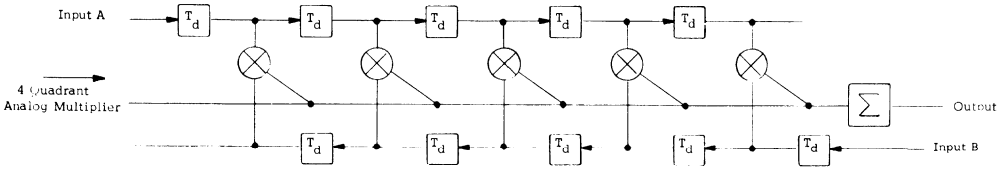
a. Fixed Binary Signal



b. Fixed Analog Signal



c. Variable Binary Signal



d. Second Analog Signal

Figure 2. Comparison of Various CTD Structures

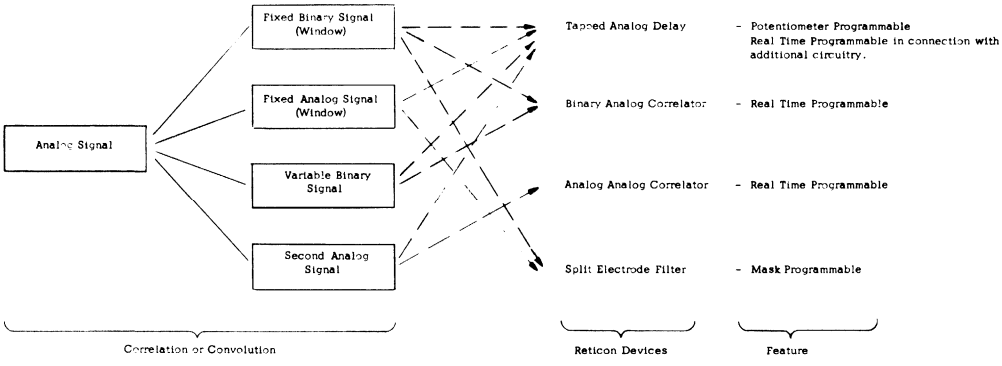


Figure 3. CTDs for Various Kinds of Analog Signal Processing

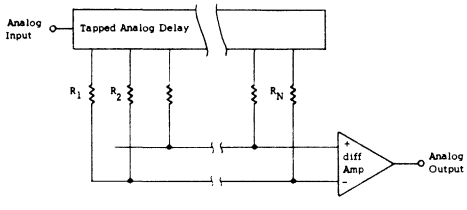


Figure 4. Tapped Analog Delay

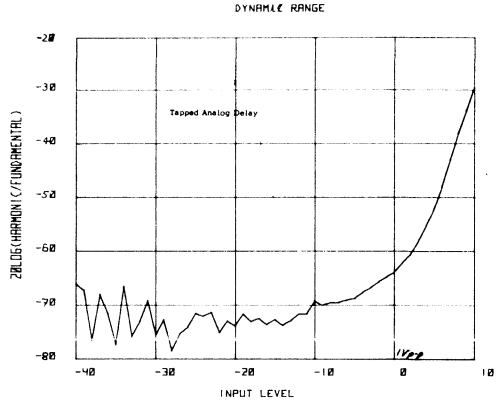


Figure 5. Harmonic Distortion of Tapped Analog Delay

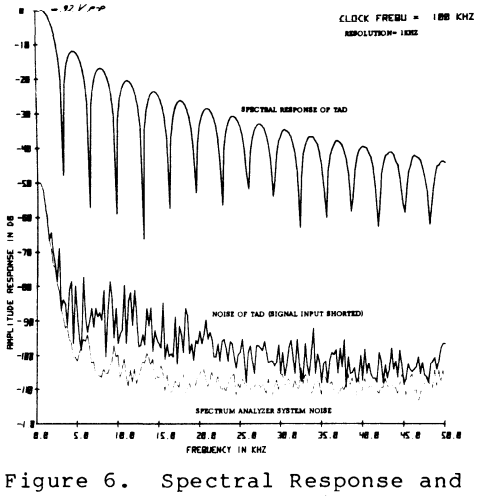


Figure 6. Spectral Response and Spectral Noise of Tapped Analog Delay with Rectangular Window

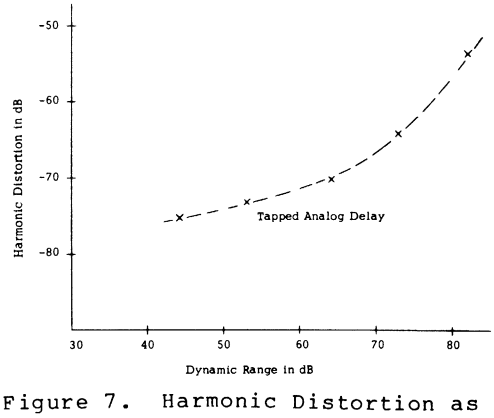


Figure 7. Harmonic Distortion as a Function of Dynamic Range in Tapped Analog Delay

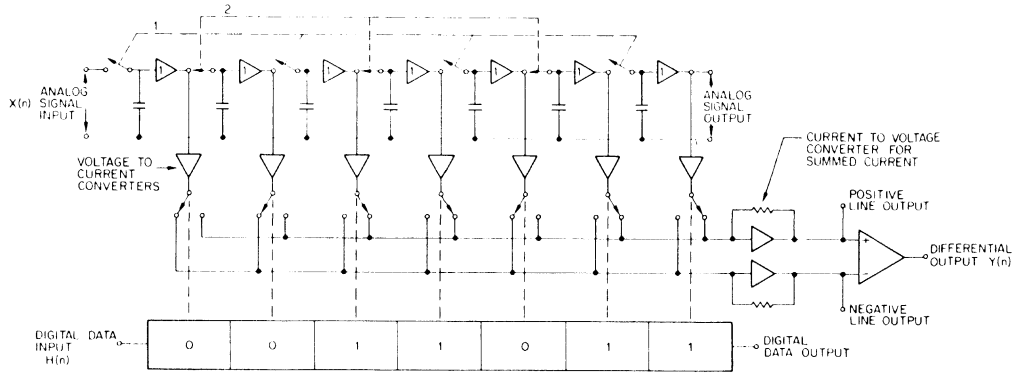
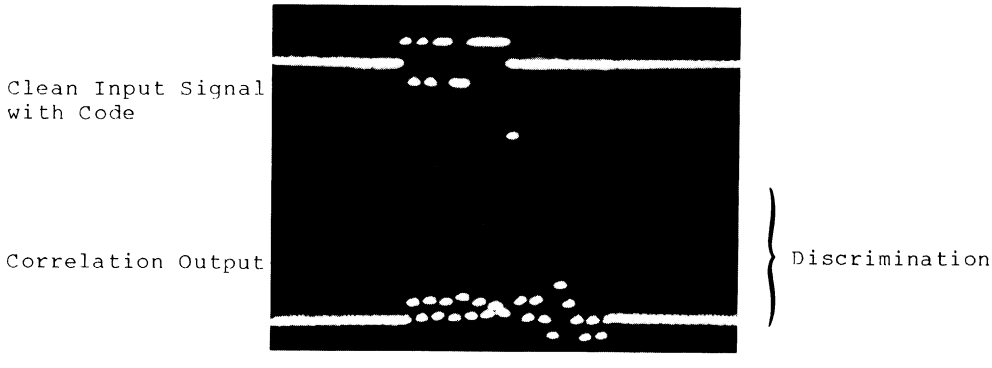


Figure 8. Binary Analog Correlator



a) Input Signal contains code only

b) Code in Input Signal is buried in noise

Figure 9. Correlation Output Obtained by Correlating Signal with High Discrimination Code with Same Code Stored in Digital Shift Register

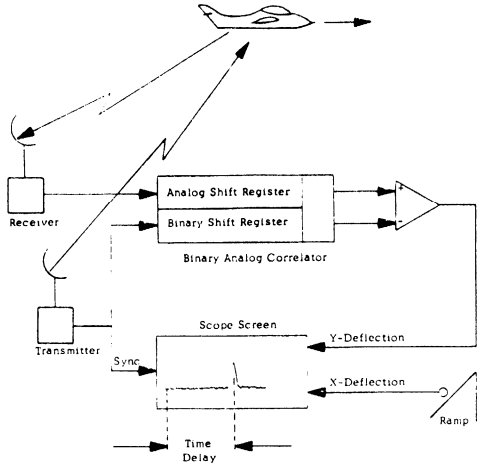


Figure 10. Radar Application for Binary Analog Correlator

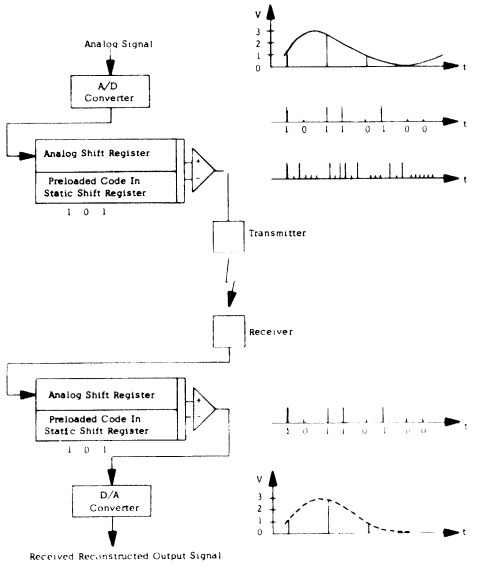


Figure 11. Binary Analog Correlator Used in Spread Spectrum Communication System

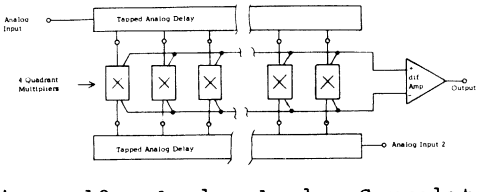
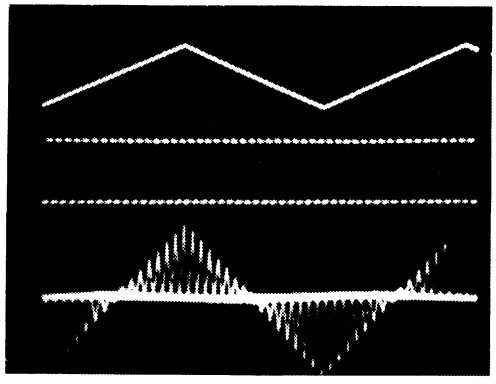


Figure 12. Analog Analog Correlator



1 Volt/Div.

1 Volt/Div.

100 mv/Div.

2 ms/Div.

$$f_{SAMPLE} \sim \frac{1}{5.4} \times 10^6$$

$$= 185 \text{ KHz}$$

Figure 13. Demonstration of Convolution/Correlation Performed by Analog Analog Correlator

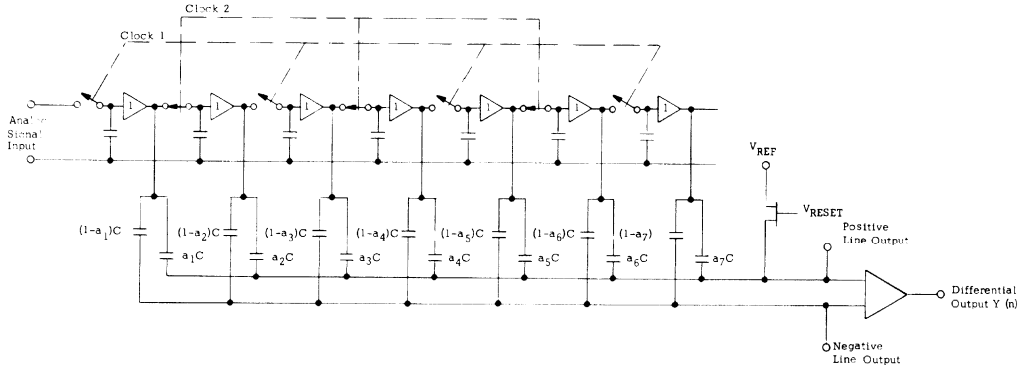
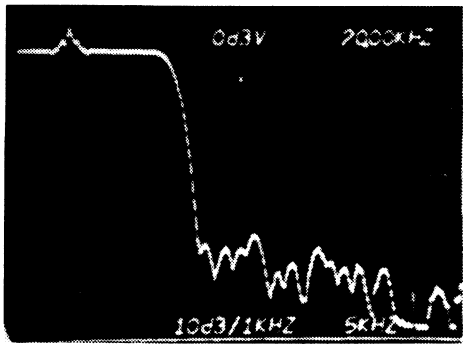
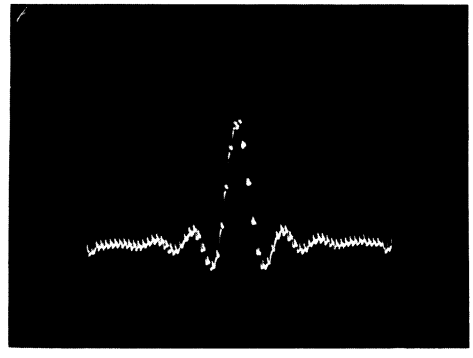


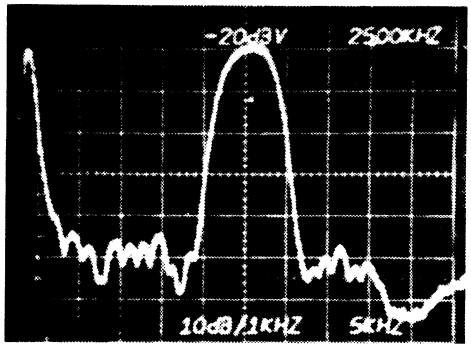
Figure 14. Transversal Filter with Split Electrode Structure



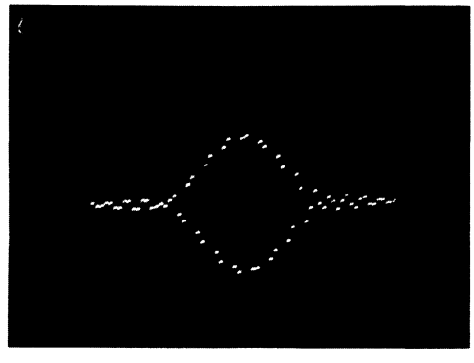
Low Pass



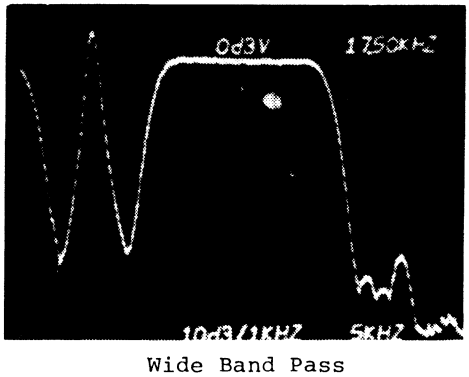
Low Pass



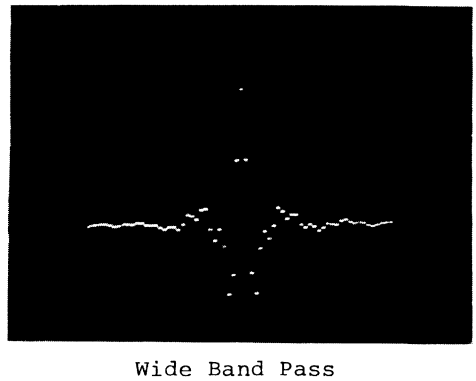
Narrow Band Pass



Narrow Band Pass



Wide Band Pass



Wide Band Pass

Figure 15. Spectral Response of Different Transversal Filters (Clock Frequency = 100 KHz) (High spikes are caused by Spectrum Analyzer d.c. Response.)

Figure 16. Impulse Response of Transversal Filters of Figure 15

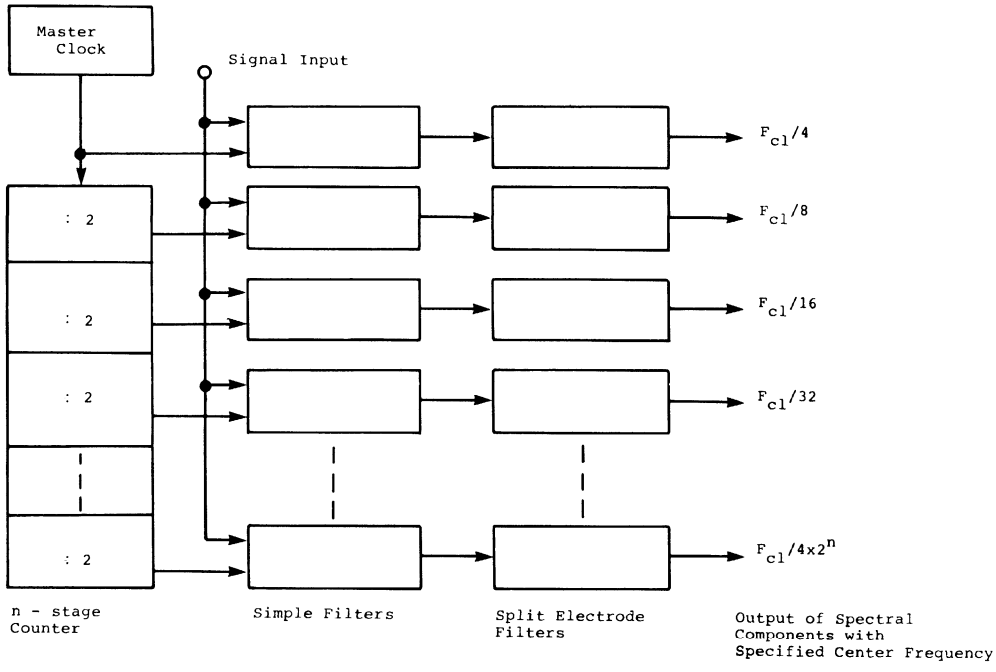


Figure 17. Spectrum Analyzer Using Transversal Filters

A TIME BASE COMPRESSOR FOR LOW FREQUENCY CHIRP-Z TRANSFORMS

APPLICATION NOTE NUMBER 115

Introduction: The RC5601 Chirp Z Transform (CZT) module supplied by Reticon provides real time spectral transform data at rates from 1KHz to 200KHz. Resolution is a function of the system clock rate since the R5601 device is only of the finite length of 512 points. Various low-frequency spectrum-analysis requirements exist; however, low-frequency transforms suffer from degradation due to thermal dark current spilling into the discrete signal samples stored in the R5601 delay line. One solution to go to lower clock rates is to provide external cooling since leakage current decreases by a factor of two for each $7^{\circ}C$ reduction in substrate temperature. Since this may be cumbersome to implement, the alternative approach is to use time base compression (TBC) of all the input data to be analyzed. TBC entails recording data (storage in a memory) at a suitable sample rate and then playing it back at a much faster rate (memory readout). This can be accomplished simply with low-cost digital memories as will be shown in this application note.

I. Implementation:

The approach discussed here will be the 'ping-pong' memory structure seen in Figure 1. An analog signal, suitably bandlimited, is sampled at a rate given by the user clock. Each signal sample is written into either MEM1 or MEM2 depending on which position the multiplexer switch selects. At the same time MEM1 is being filled, MEM2 is being emptied, but at a much higher rate given by CLK H. Once MEM2 is completely read, the output MUX switch moves to position 3 designated the idle position. Of course MEM2 will finish its cycle sooner than MEM1 can due to the higher clock rate MEM2 operates at. When MEM1 is filled the input MUX SW switches to position 2 and the output MUX SW switches to position 1. Now MEM1 is read back at the CLK H rate while MEM2 fills with the next set of data samples at the user clock rate, CLK L. Graphically, the effect of time base compression can be seen in Figure 2. Physically, the speedup of playback extends the bandwidth of the original input signal by a factor K, the ratio of the read out to read-in clock frequencies.

An additional requirement imposed by the nature of the chirp-z transform is that the input data must be periodic. A simple way to ensure this is to simply repeat the playback of the record that loads the R5601. During the second playback, the transform is valid.

Figure 3 shows a more detailed block diagram of the TBC circuit. This implementation uses RAM's as the memory. Tristate data buffers are enabled when data from the A/D converter is written into the memory. An output multiplexer selects either memory for playback and directs the data into a latch which drives the D/A converter. All functions are controlled by simple logic gates and flip flops. In operation, the memories are gated as shown in the simplified timing diagram.

II. Applications:

Any general low frequency Fourier analysis can be performed with its CZT module and its TBC. Some areas of applications are as follows:

- Seismic data reduction (on site FFT analysis).
- ECG spectrum analysis in real time.
- EEG spectrum analysis in real time.
- Vibration control and measurement spectral information.
- Sonar signal signature spectra.
- Machinery health monitoring.
- Tape recorder wow/flutter or record warp spectra measurement.

III. Performance:

The system dynamic range is limited by the quantization noise to 48dB which is due to eight bit encoding. No improvement in the output spectrum noise floor is evident so the CZT card dynamic range of $\approx$ 40dB is maintained. The TBC adds the flexibility of performing the true conventional CZT instead of the sliding CZT. This offers the advantage of better transform accuracy of non stationary waveforms such as a heartbeat pulse or a dolphin sonic burst. With windowed chirp ROM's, a problem for transient signals exists in that a short term transient may be windowed out if it occurs at the very start or end of a write record. It is suggested that for such signals, a delay can be added so that they get multiplied by the peak of the window function which occurs half way through a written record.

The card as designed will accept user clock rates down to 1Hz and is limited by droop in the input sample and hold. Readout data rate is 125KHz and can be dropped to 2KHz by stringing additional counters at the shift register (2G11) output (Figure 4). The system resolution at 1 Hz is .004 Hz in a total signal bandwidth of 1/2 Hz.

Interface:

Many applications require spectra averaging or spectral line selection for setting the analyzer Q or bandwidth. Such post processing operations can be done digitally and, to access the CZT output approximately, an A/D converter would have to be synchronized to the output sweep. An appropriate trigger pulse is available at the CZT ROM address counters as the clock line goes through low toward the end of the CZT output samples.

Input levels to the TBC can be as high as 10 volts peak to peak. For greater sensitivity, the gain of the output DAC can be increased by increasing the values of the resistors used in the output op amp buffer. Power requirements are ±15 volts @ 100mA and +5 volts @ 1.2 amp. It is suggested that in a fully integrated system (CZT module with TBC card) larger regulators replace the present devices used on the CZT module so that the TBC card can be powered with the same.

Timing Diagram Description (Figure 9)

In Figure 9, data is always being written into one of the memories, accordingly W1 (write into 1) and W2 (write into 2) are complements of each other.

The length of time W1 is high is equal to $\frac{512}{\text{frequency of user clock}}$

or equivalently, 512 samples at the user clock rate.

The read time from a memory takes 8.1 msec determined by $\frac{(512 \times 2)}{\text{CZT Clock}} = \frac{1024}{125\ \text{KHz}}$.

This is two playbacks of the 512 word record written into the memory.

Since the memory is split into two 256 word blocks, chip enable (CE) must be toggled twice. During a memory write, only a single toggle of the chip enable line occurs except when data is being written during which the write enable pulses occur.

Generation of the system reset pulse occurs each time a W1 (or W2) transition occurs. The memory write enable (WE) clocks a flip flop which latches a terminal count (512th address present) for the ending write cycle.

When reset goes low, the system clock is disabled so the CZT board doesn't take in any analog data until the next user clock pulse occurs.

Analog Card Description (Figure 4)

This card provides analog/digital (A/D) conversion and D/A conversion as well as the master clock. Figure 4 shows the schematic diagram of the analog card. U1 takes a 3 usec sample of the analog signal when the S/H command line goes high. Approximately one-half usec later, the A/D strobe line goes high (See Figure 8, timing diagram) which resets the successive approximation register, U5, running off its own 5 MHz clock (U6). The register sequences through the eight possible bit values and upon decision by comparator U4, holds a one or a zero for a particular bit. The decision is made for the analog input compared to the equivalent analog value of the eight bits which is generated by a D/A converter, U3. After eight clock periods, $\approx$1.6 usec, the data is stable and is available to the TBC memory. Data is formatted as an 8 bit PCM code in standard binary.

Data read from the TBC memory is converted back to analog by U7 and U8. The gain of this section is one tenth so that a ten volt (11111111 count) binary input will generate a one volt analog output for the CZT input.

Master oscillator U11 generates a 4MHz clock for the TBC timing and control. P2 sets the free running frequency.

Voltage regulators U9, and U10 stabilize supply variations for the oscillator and generate the required -5 volts for comparator U4.

A 10 volt reference from U2 matches the reference input currents for the DAC-08's U3 and U7.

P1 and P3 are offset adjustment pots. P1 is set to offset the analog input signal by +5 volts. This is the equivalent of converting the standard binary data output into offset binary where 10000000 represents 0 volts, 00000001 represents -10 volts and 11111111 represents +10 volts. P3 removes any DC offsets from U7 and U8.

All the analog circuitry uses an isolated analog ground to keep noisy digital signals from affecting the A/D converter performance. The components fit on a 4.25" x 2.9"card which plugs into the wire wrap card containing the digital IC's.

Compressor Logic Description (Figure 4)

The user clock is shaped into a 1 usec pulse by a one shot (7B) and sent to the clock multiplexer (5F). Another one-shot (7B) generates a 3 usec pulse for the sample and hold on the analog card. A 4 MHz clock generated on the analog card is divided by two (7G) and sent to a divide by 16 circuit composed of a shift register (2G) and gates (3G). This becomes the CZT clock at 125KHz which can be interrupted during system reset. Also a delayed CZT clock is available by choosing a particular Q output.

Another shift register (1G) is used to generate the A/D convert command and the write enable (WE) by a combination of the Q outputs with 'and' gates (6G). Write enable must meet the RAM setup requirements.

All eight bits of data are written or read simultaneously depending on the mode the system is in. During W1 (write into memory 1) data buffers (7E) and (7F) are enabled only when WE goes low. Chip enable for (B) & (C) is low for the first 256 words while CE for 5B and 5C is low for the next 256 words. Counters (6D) and (5D) reverses the chip enables through a J-K flip flop (6F). (6E) functions as a divide by 2 and generates a TC after 511 words. Logic gates (4D) and (3A) toggle flip flop (6F) when the next WE pulse occurs. W1 then goes low and W2 is high. When W1 goes low, flip flop (2A) latches a one and R1 goes high. Now memory one is in read while memory two is in write.

During R1, clock MUX (5F) gates in the CZT clock from (2G) after the reset line goes high. Now the address counters clock through 256 words, toggle the chip enables, then the same sequence is repeated until 1023 playbacks have occurred. A delayed CZT clock from (2G) clocks the data latches (1B) and (1C). J2 and J4 act as on-off gates for the data. In the off condition, a code of 10000000 is presented which converts to 0 volts at the D/A converter output. When TC2 from (5E) goes high then the last word is read. R1 goes low to disable any further address advance and memory 1 sits in an idle mode until W2 goes low. MEM2 sequences in the same manner as MEM1.

Additional logic gates (J7) and (J5), and flip flop (J3) detect the first half of R1 or R2 to act as a squelch during that time. When the second half of R1 or R2 occurs, the CZT analog output is valid and the squelch circuit composed of analog gates (SD 5000) passes the CZT output.

(4A) is a switch pak which sets the preset bit values for the ÷ N counter used to determine the number of read records. The playback settings are:

P0	P1	P2	P3	
0	0	1	1	1 RECORD
0	1	0	1	2 RECORDS
0	0	0	1	3 RECORDS
0	1	1	0	4 RECORDS
0	0	1	0	5 RECORDS
0	1	0	0	6 RECORDS
0	0	0	0	7 RECORDS

Additional control lines called WLCONV and TMON and START WRITE were formerly used for a transient monitor mode which was found to be unsuccessful when windowed chirp ROM's were used.

A manual and power-on reset are made by using a NAND schmidt trigger, (1E).

CZT Board Modifications

6

The master oscillator, U5 is removed since the CZT card will be slaved to the TBC. In its place, a strip of seven wire wrap pins were inserted where pins 2 to 8 used to be. The connections made to the prototype are as follows:

2	GND
3	RESET
4	GND
5	MASTER CLOCK
6	NC
7	TC FOR U8
8	GND

Steps for modification:

1. Remove U5.
2. Cut trace from pin 1 of U8 to pin 3 of U8.
3. Connect pin 1 of U8 to pin 1 of U9.
4. Connect pin 4 of U4 to pin 7 of U5. (pin strip).
5. Connect pin 3 of U5 to pin 14 of P5. (in sync line).
6. Connect pins 2 and 4, to pin 8 of U5.

A molex connector makes a convenient plug for the wire wrap pins. In the prototype a cable with molex pins on both ends was used to connect the two boards.

One additional change is required in the ROM's used to generate the pre-chirp multiplication on the CZT board. At the end of a record playback, usually the last sample is different from the first in amplitude. Since the conventional CZT requires the repeat playback of the input data, an abrupt transition occurs at the start of the second playback. This discontinuity causes the CZT output to have "frequency leaks". These leaks are actually sidelobes of the sin x/x function.

The spreading of the CZT output can be prevented by windowing the input data such that at the start and end of the record, the amplitude goes smoothly to zero or very close to zero. A Hanning window has the functional form of a raised cosine pulse. i.e., $W(n) = .54 - .46 \cos \frac{2\pi n}{N-1}$ Where N = 512 in this case.

The ROM's used on the CZT module were modified to include the Hanning window. With windowed chip ROM's, the CZT requires an unwindowed chip filter, i.e., the R5601-1.

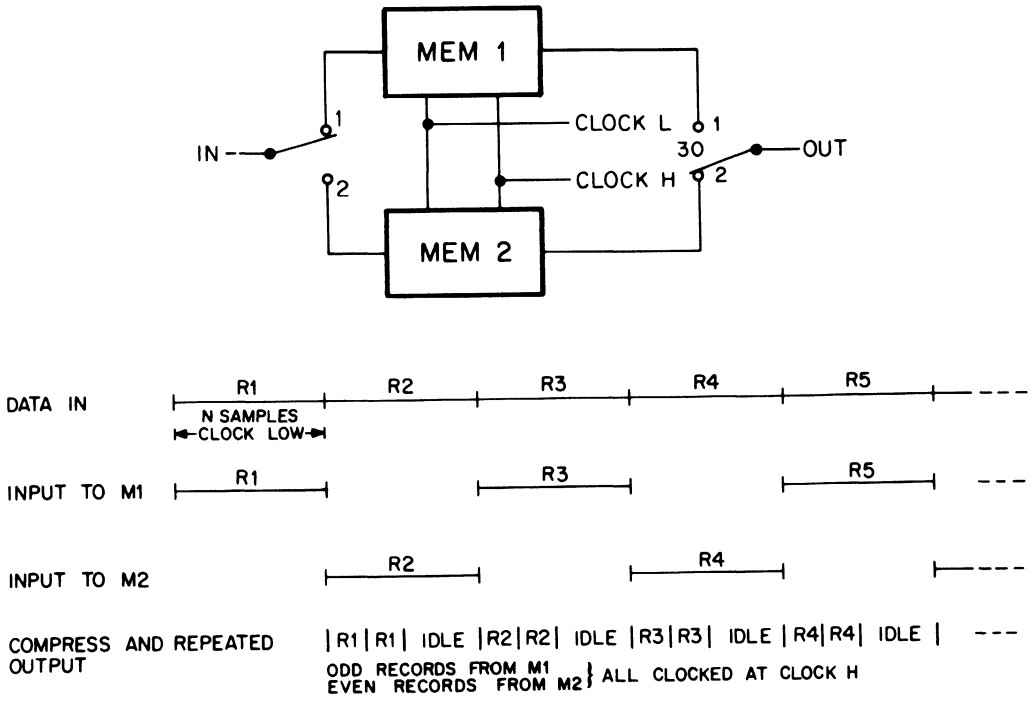


Figure 1. "Ping Pong Memory"

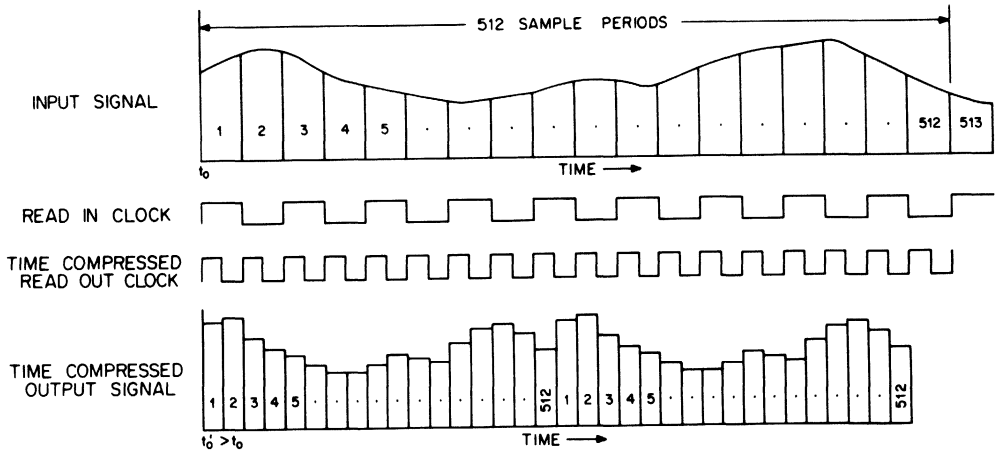


Figure 2. Time Base Compression

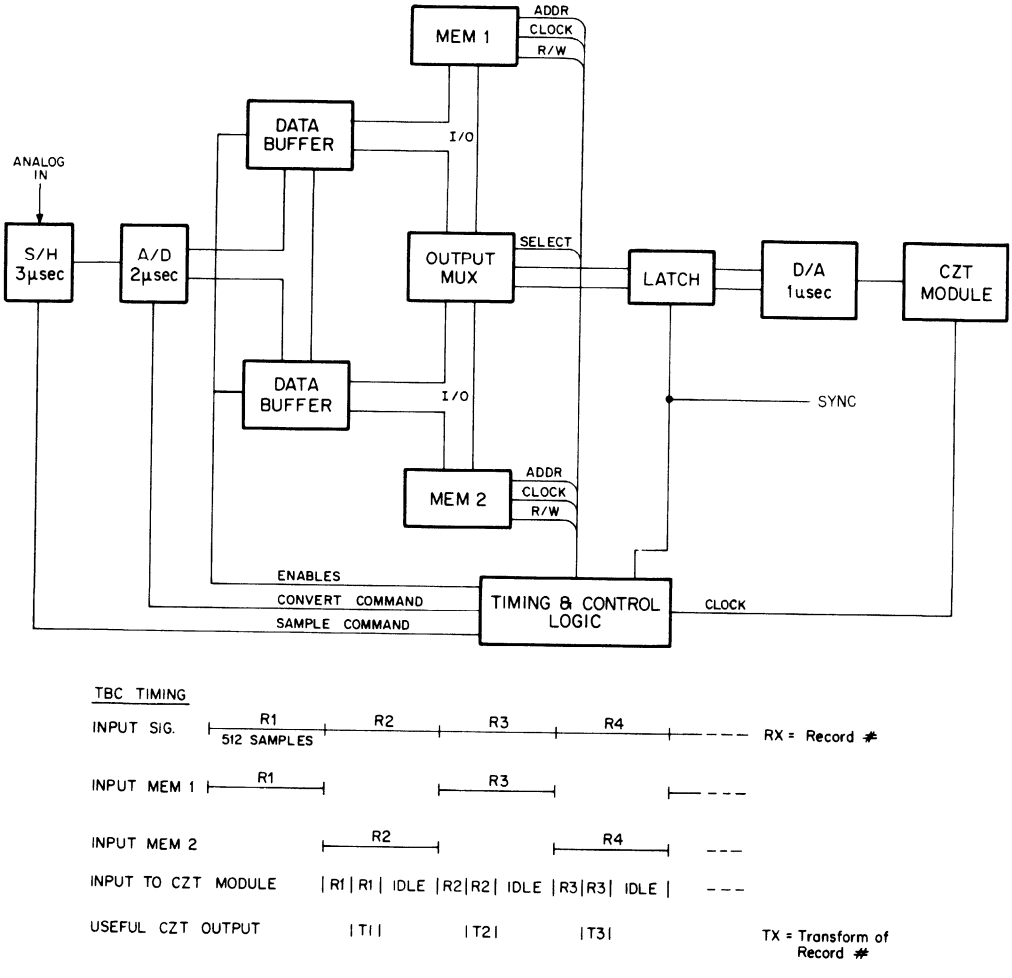


Figure 3. Block Diagram Implementation on the Time Base Compressor

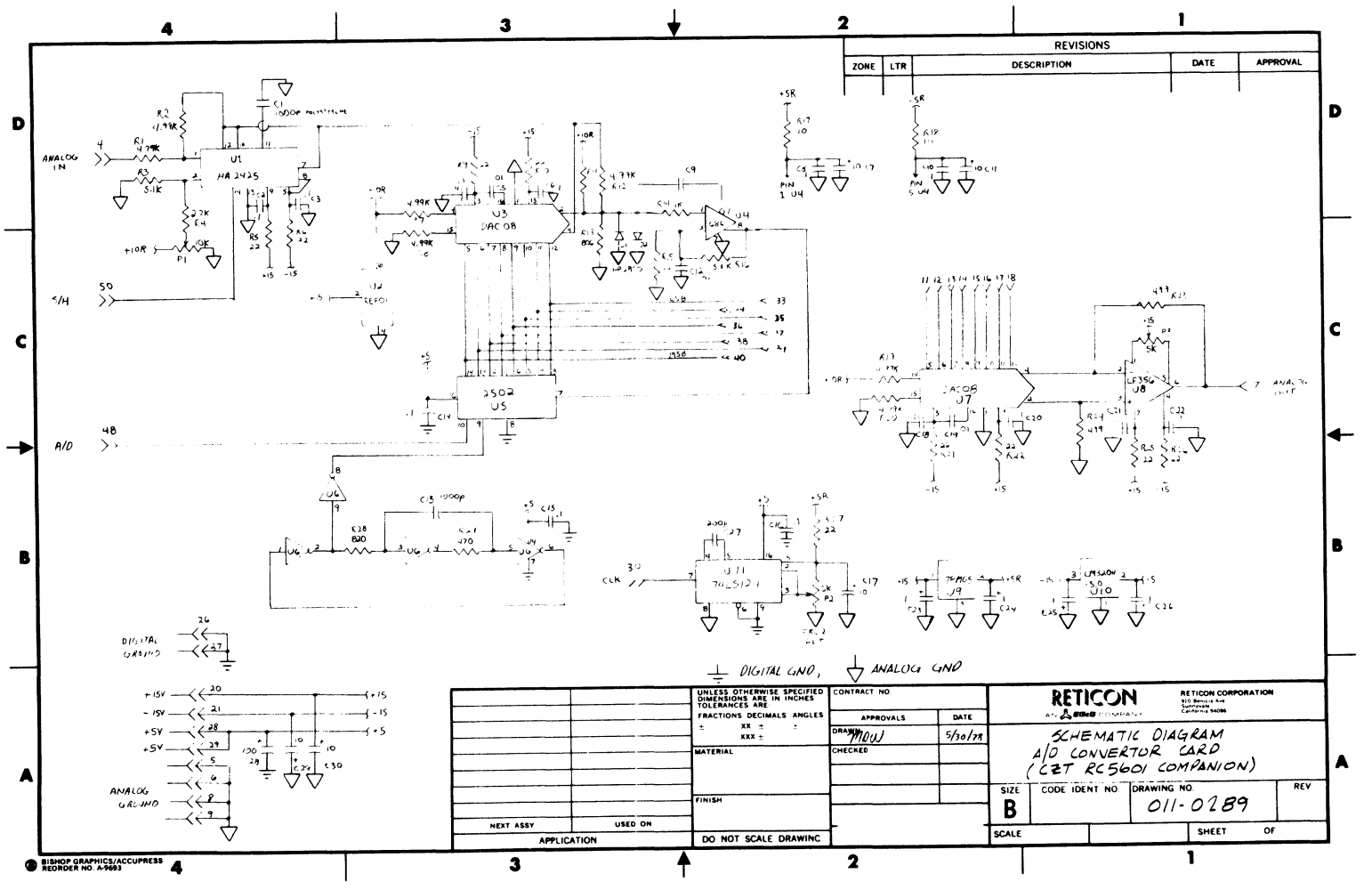


Figure 4. Schematic Diagram A/C Converter Card

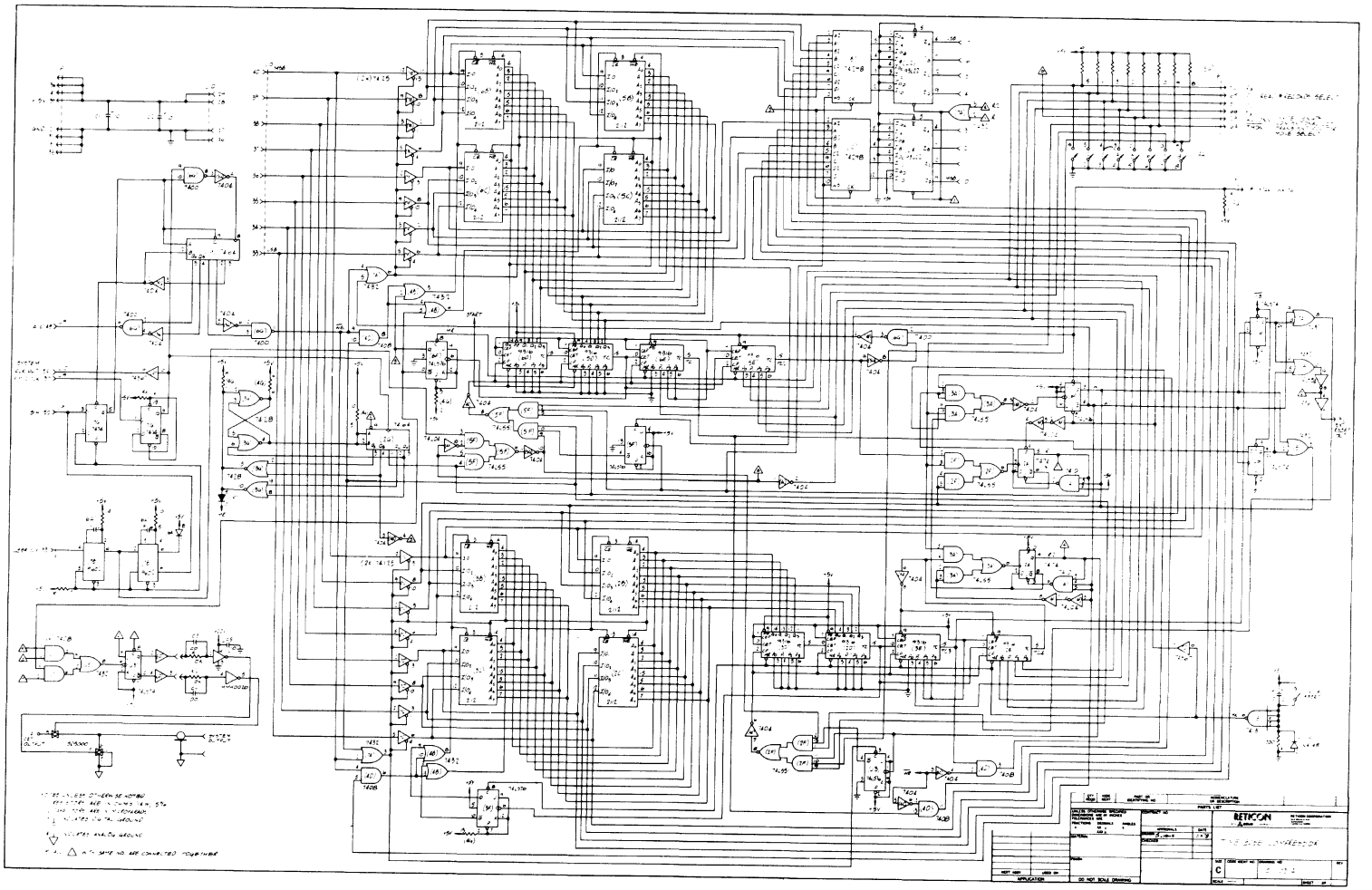


Figure 5. Time Base Compressor Diagram

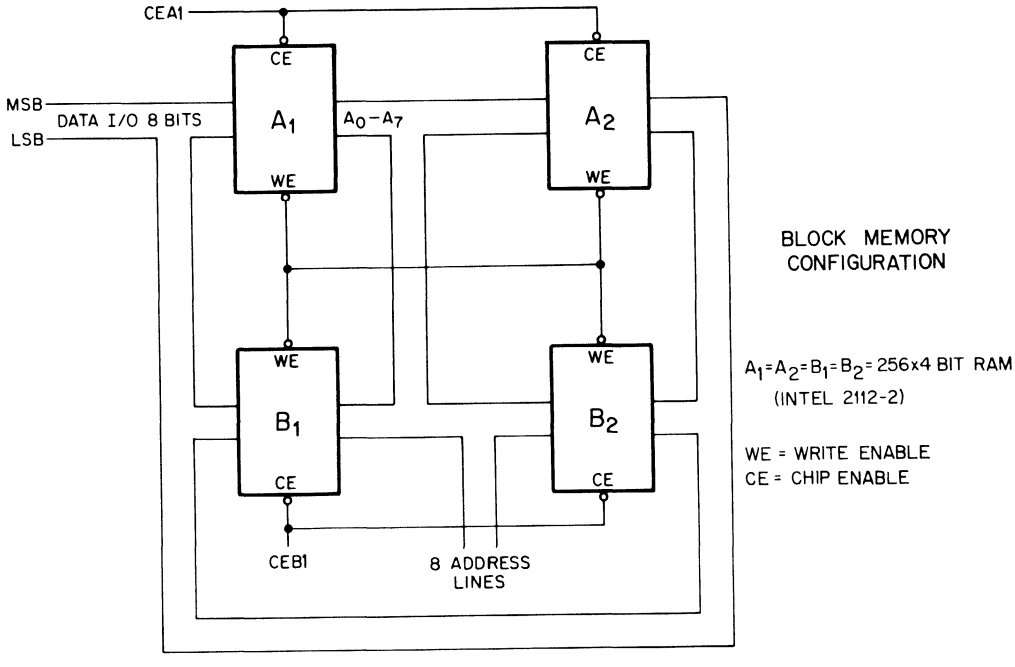


Figure 6. Memory Configuration

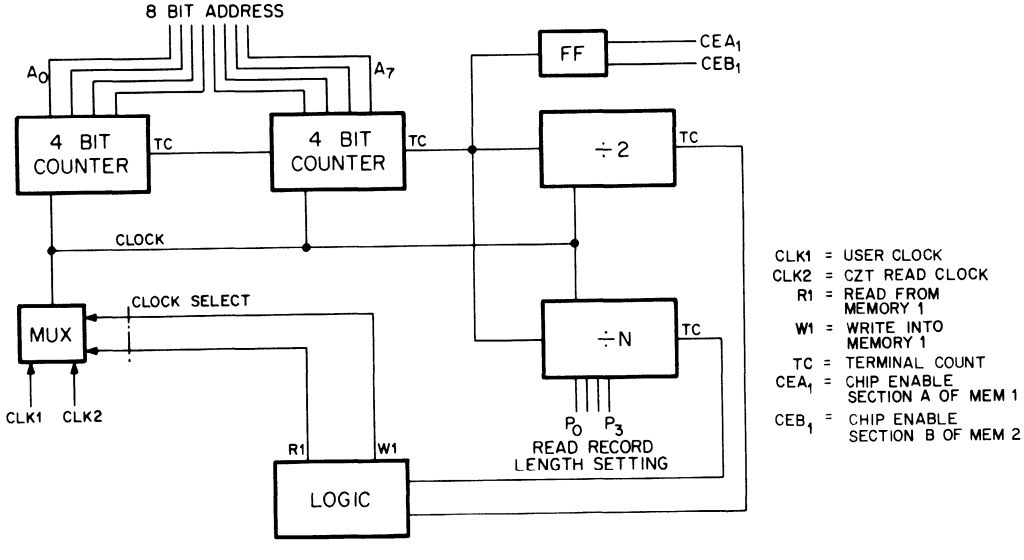


Figure 7. Memory Address Scheme

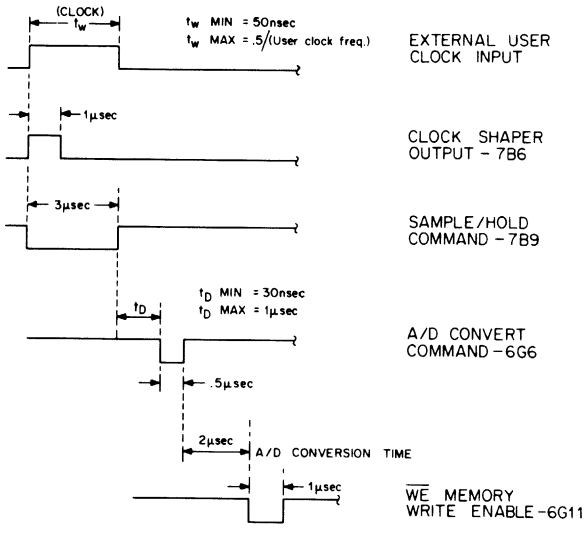


Figure 8. Single Write Cycle Timing

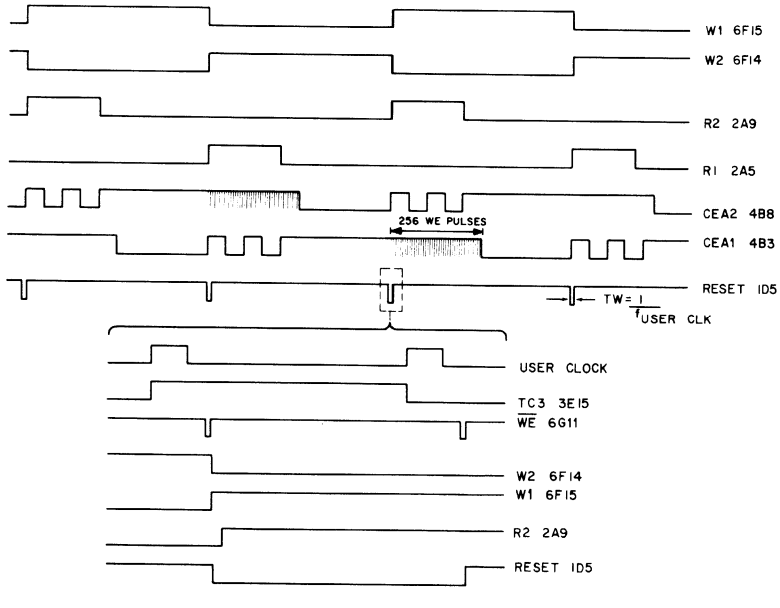


Figure 9. Major Timing Waveforms

New products

Active filter is configured digitally

Universal switched-capacitor filter IC in 18-pin DIP needs neither calculations for use nor external components

by Stephen W. Fields, Palo Alto regional bureau manager

The best thing about a new universal active filter from Reticon Corp. is that it's not necessary to be a filter designer to use it. There are no equations to figure out since there are no external components both the frequency and the Q are set digitally.

Designated the R5620, the n-channel MOS integrated circuit is a second-order switched-capacitor filter network capable of implementing the five basic filter types—low-pass, high-pass, bandpass, notch, and all-pass—without any external components other than a clock.

The different filter types are selected by strapping three pins in various combinations. Next, the Q and the center-frequency response are selected. This is accomplished with 10 pins: five select the ratio of the clock frequency to the center frequency over a two-octave spread from 50 to 200 in 32 logarithmically spaced increments, and five select the Q value from 0.57 to 150 in 32 steps. Center frequencies range from 0.5 Hz to 25 kHz, and the clock rate can be from 10 Hz to 1.25 MHz.

According to Douglas Cox, the designer of the R5620, the Q values were selected to easily implement classic low-pass filters as well as the most common bandpass filters. "And the center frequencies are equally spaced in terms of per cent so that we get essentially the same accuracy over two octaves," says Cox, adding that this is important in tracking filter applications.

Real-time filter change. The parameters may be selected by hard-wiring the appropriate pins or through digital control by external logic circuits. "With digital control," says Cox, "you can actually change the filter's characteristics in real time, on the go."

The key to the filter's simplicity, says its designer, is that "with most other universal active filters, there is one input and three outputs to get the required function—they need an op amp summer to produce the desired filter characteristics. With our design, the filter type is selected by configuring the inputs, and we only have one output so we don't need an external op amp."

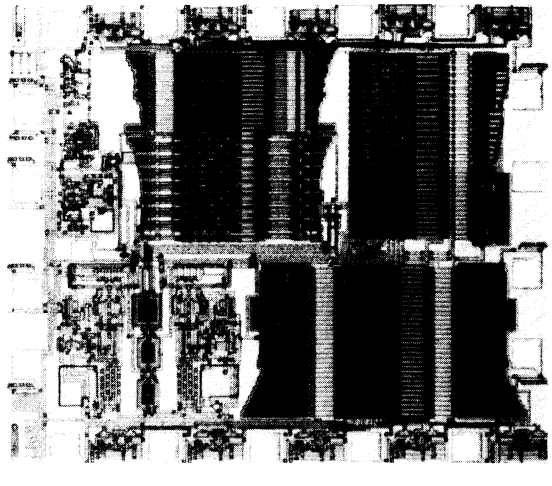
Switched-capacitor techniques were used in the design, according to Cox, as they are a good way to implement a resistor. "Integrated-circuit resistors take up a lot of area and they are not very accurate. But with capacitors, we use the ratio of one to another, and we can get better than 1% accuracy. And with MOS op amps, we don't need much current, so the capacitors can be small."

Switched-capacitor filters are actually traditional active filters with switched-capacitor resistors in place of the normal nontunable resistors. Because such filters are very stable and can be tuned by varying the master-clock frequency, alignment problems and the need for tight-tolerance components and trimmer potentiometers are eliminated.

The R5620 requires from ±4 to ±11 V; supply current is typically 4.5 mA, and the maximum output current is 4 mA. Output voltage swing is 14 V peak to peak. Output noise is typically 270 μV with a Q of 1, and the filter has a dynamic range of 94 dB with a Q of 1 and 84 dB with a Q of 40. Total harmonic distortion at 1 kHz is typically 0.2%.

Available from stock, the R5620 in an 18-pin plastic dual in-line package is priced at $10 each in quantities of 100. In volume orders of 10,000 pieces, it is under $5.

Reticon Corp., a subsidiary of EG&G Inc., 345 Potrero Ave., Sunnyvale, Calif. 94086. Phone (408) 738-4266 [338]



Notes

Notes

Notes

Analog Signal Processing Products

Reprints

Switched-Capacitor Techniques Implement Effective IC Filters

A. M. Davis

Monolithic Filters for 1200 Baud Modems

Lyon T. Lin
Hsin-Fu Tseng
Les Querry

A Monolithic Audio Spectrum Analyzer for Speech Recognition Systems

Lyon T. Lin
Hsin-Fu Tseng
Douglas B. Cox
Ronald G. Runge
Denton P. Conrad

A Low Speed Switched Capacitor Modem Filter I.C. That Is Compatible With the C.C.I.T.T. V.21 Modem

Cecil W. Solomon
Douglas B. Cox
Michael G. Gabler
Udo Strasilla

A Mask Programmable SCF and Logic Array for Semi Custom Analog System Integration

Tsung D. Mok
Peter A. Ateshian
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A Digitally Programmable Switched-Capacitor Universal Active Filter/Oscillator

Douglas B. Cox

Switched-capacitor techniques implement effective IC filters

Adding to the repertory of available analog building blocks, integrated filters utilizing switched-capacitor methods simplify analog designs.

A M Davis, San Jose State University

Filters using switched-capacitor techniques overcome a major obstacle to filter-on-a-chip fabrication—the implementation of resistors—by simulating resistors with high-speed switched capacitors. Such an approach thus eliminates the necessity for precise integrated-resistor values—a requirement previously met only by hybrid devices that require costly trimming procedures—and permits fabrication of precise monolithic analog capacitor filters.

Although filters other than switched-capacitor types can also be effectively integrated, they present problems that limit their usefulness. Sampled-data filters such as CCD and bucket-brigade devices, for example, suffer from a low S/N ratio and a need for complex postfilter antialiasing because of their low sampling rate compared with filter bandwidth. Digital filters also suit integration processes, but their complexity and stringent clock-rate requirements currently prevent their consideration as general-purpose filters (although they are becoming more attractive for specialized applications).

As an alternative to these designs, then, switched-capacitor (SC) filters combine many of the advantages provided by digital filters with those of their purely analog counterparts. This article outlines SC filters' advantages by examining these devices' basic operating theory and some of their practical limitations, and by developing two SC filter types.

Substitute capacitors for resistors

An SC consists basically of a capacitor whose charge is transferred from one node to another by a switch. In position 1 (as shown in **Fig 1**), the switch allows C_s to charge to $Q_1=C_sV_1$; in position 2, it discharges to $Q_2=C_sV_2$. An amount of charge equal to $\Delta Q=Q_1-Q_2$ therefore transfers from terminal 1 to terminal 2.

If the switching period is T, this charge transferral represents an equivalent current of

$$I = \frac{\Delta Q}{T} = \frac{V_1 - V_2}{\left(\frac{1}{C_s}\right)T},$$

and the form of this equation indicates that the switched capacitor can be modeled as a resistor of value $R_{eq}=1/f_sC_s$, where $f_s=1/T$ is the switching frequency.

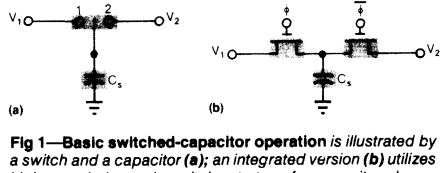

Fig 1—Basic switched-capacitor operation *is illustrated by a switch and a capacitor* **(a)**; *an integrated version* **(b)** *utilizes high-speed electronic switches to transfer capacitor charge from V_1 to V_2, thus simulating a resistor.*

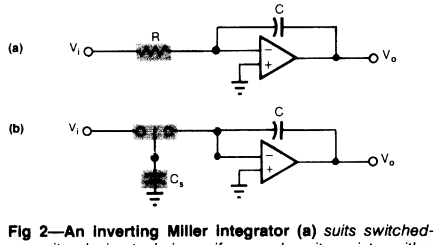

Fig 2—An inverting Miller integrator (a) *suits switched-capacitor design techniques if you replace its resistor with a switched capacitor* **(b).**

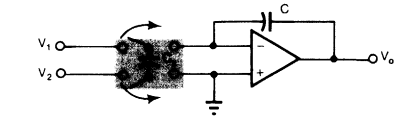

Fig 3—A differential integrator *is easy to construct using switched-capacitor methods. The arrows indicate switch phasing.*

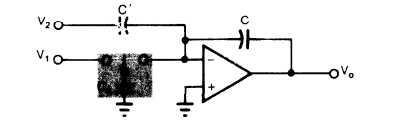

Fig 4—An integrator/summer *allows you to add as many summing inputs as required.*

Precise MOS-IC capacitors substitute for filter resistors

This analysis involves two implicit assumptions. The first lies in relating charge transferral in discrete quantities to current—a relationship that holds only for high sampling rates. But SC filters do in fact utilize high rates to avoid complex analog antialiasing and postfiltering. The second assumption is that the voltages V_1 and V_2 are independent of the transferred charge. The SC integrator to be presented here does indeed implement such a charge-independent circuit.

Construct a switched-capacitor integrator

To understand SC integrators, consider the inverting Miller integrator shown in **Fig 2a.** This common analog-design tool's transfer function is

$$H(j\omega) = \frac{-1}{j\omega RC}.$$

The SC integrator shown in **Fig 2b** replaces the Miller circuit's resistor with a switched capacitor and provides the transfer function

$$H_{sc}(j\omega) = \frac{-1}{j\omega\left(\frac{C}{f_s C_s}\right)}.$$

Examining these integrators' gains makes the advantages of switched capacitors clear. The analog integrator furnishes a gain equal to 1/RC—a factor that determines such parameters as bandwidth or peaking frequency in active-filter circuits. But the SC integrator's gain equals $f_s C_s/C$—an advantage, because MOS IC technology can implement capacitor ratios to within about 0.1% of specified values (an impossible figure for resistor values to match). The switching frequency f_s isn't difficult to supply with similar precision, so the SC method allows very precise gain specifications without trimming. In addition, you can vary the circuit's gain (and thus tune the filter) by changing f_s.

Utilizing switched capacitors, you can also easily construct a differential integrator **(Fig 3)**—a relatively difficult enterprise in conventional analog form. This integrator differs operationally from the single-switch version in only one way: The differential circuit charges C_s to $V_1 - V_2$ rather than to a single input voltage, resulting in an output voltage given by

$$V_o = \frac{-1}{j\omega\left(\frac{C}{f_s C_s}\right)}(V_1 - V_2).$$

The filter circuits presented later in this article capitalize on this important relationship.

One other circuit that deserves attention is the integrator/summer **(Fig 4).** Analyzing this circuit by superposition shows that

$$V_o = -\frac{-1}{j\omega\left(\frac{C}{f_s C_s}\right)} V_1 - \frac{C'}{C} V_2;$$

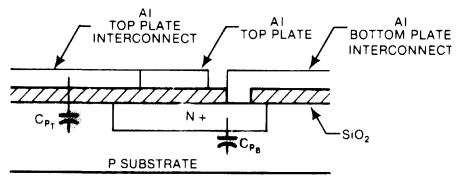

Fig 5—An MOS capacitor *contains two major parasitic-capacitance areas: between the top plate and substrate and between the bottom plate and substrate.*

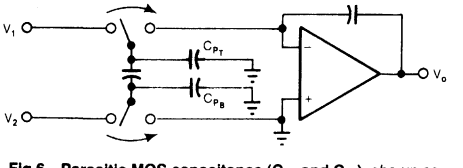

Fig 6—Parasitic MOS capacitance (C_{PB} and C_{PT}), *shown as it would appear in a circuit, either harmlessly discharges to ground (C_{PB}) or is too small to greatly affect circuit performance (C_{PT}).*

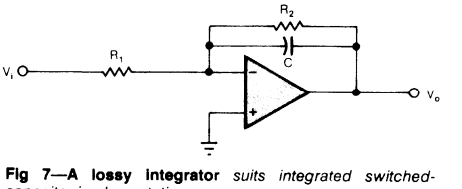

Fig 7—A lossy integrator *suits integrated switched-capacitor implementation.*

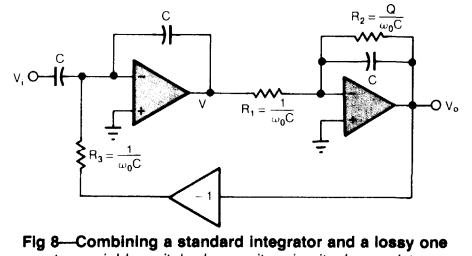

Fig 8—Combining a standard integrator and a lossy one *creates a viable switched-capacitor circuit when resistance values are stated in terms of capacitance and switching speed.*

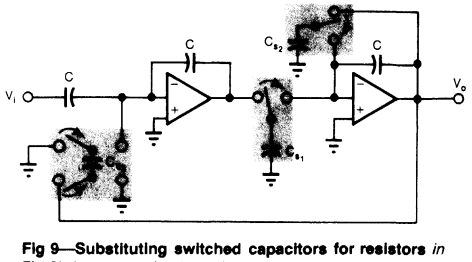

Fig 9—Substituting switched capacitors for resistors *in Fig 8's integrator circuit produces a precise, easily integrated filter.*

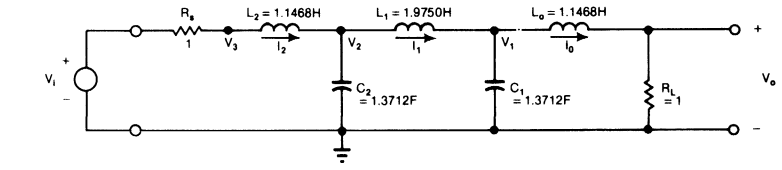

Fig 10—A fifth-order Chebyshev low-pass filter *constitutes a switched-capacitor arrangement that exhibits low sensitivity to its inductor and capacitor values in the passband. (Impedance or frequency scaling of components is not necessary at this initial stage.)*

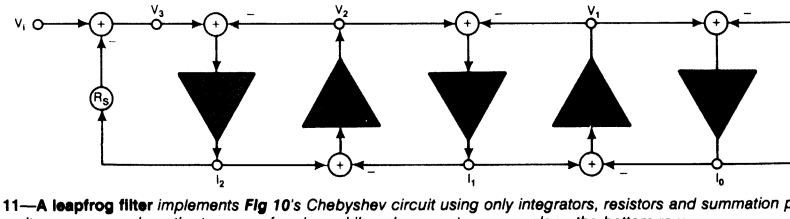

Fig 11—A leapfrog filter *implements Fig 10's Chebyshev circuit using only integrators, resistors and summation points. Note that only voltages appear along the top row of nodes, while only currents appear along the bottom row.*

the circuit allows straightforward extention to any number of summing inputs.

The theoretical circuits just described can't be perfectly implemented, of course. An MOS capacitor, for example, incorporates inherent parasitic properties, primarily between its bottom plate and substrate (**Fig 5**). The bottom-plate parasitic capacitance, C_{PB}, varies between 5 and 20% of the capacitor's primary value, while the top-plate figure, C_{PT}, varies between 1 and 0.1% of that value.

To illustrate these parasitic capacitances' impact, **Fig 6** shows how they effectively fit into a circuit. Note that C_{PB} charges from a voltage source (V_2) and discharges into ground, so it doesn't affect performance at all; C_{PT} also charges from a voltage source (V_1), but it discharges into the integrator capacitor, C. However, because C_{PT}'s value is small, it doesn't affect performance in a major way. SC differential integrators can therefore be considered high-performance circuits.

Designing state-variable filters

Basing SC-filter structures on active filters containing integrators makes switched-capacitor benefits readily available. One filter type that takes advantage of these benefits is the state-variable circuit—the generic name for several integrator-based arrangements. The particular circuit considered here involves both a standard integrator and a lossy one.

Suppose you want to design a bandpass filter with the transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}.$$

After cross-multiplying and factoring, this expression becomes

$$V_o(s)\left[s\left(s + \frac{\omega_0}{Q}\right)\right] = \omega_0 s\, V_i(s) - \omega_0^2 V_o(s)$$

$$\text{or} \quad V_o(s) = \frac{\omega_0}{s + \frac{\omega_0}{Q}}\left[V_i(s) - \frac{\omega_0}{s} V_o(s)\right].$$

Now consider a lossy integrator (**Fig 7**) whose corresponding transfer function is

$$\frac{V_o(s)}{V_i(s)} = \frac{-\frac{1}{R_1 C}}{s + \frac{1}{R_2 C}}.$$

Setting $\omega_0 = 1/R_1C$ and $\omega_0/Q = 1/R_2C$ (or $Q = R_2/R_1$) changes this function to

$$\frac{V_o(s)}{V_i(s)} = \frac{-\omega_0}{s + \frac{\omega_0}{Q}}.$$

Compare this function with the transfer function originally sought, writing the original function as it was previously developed except for sign adjustments:

$$V_o(s) = \frac{-\omega_0}{s + \frac{\omega_0}{Q}}\left[\frac{\omega_0}{s} V_o(s) - V_i(s)\right].$$

To make the conversion to SC form easier to see, utilize a feedback capacitor, C, in both the standard and lossy integrations (**Fig 8**). Note that the first op amp shown in **Fig 8** is an analog integrator/summer that provides the following output voltage:

$$V = -V_i + \frac{1}{R_3 C s} V_o = -V_i + \frac{\omega_0}{s} V_o.$$

Now convert this circuit to SC form by substituting the expression for switched-capacitor (C_s) equivalent resistance: $R_{eq} = 1/f_s C_s$. The conversion thus produces $C_{s1} = \omega_0 C/f_s = C_{s3}$ and $C_{s2} = \omega_0 C/Q f_s$ (**Fig 9**).

Note that C_{s3} connects to the circuit shown in **Fig 9** in an inverting configuration—an especially interesting arrangement because when charged, C_{s3} connects between a voltage source and ground, and upon discharge, its bottom-plate parasitic capacitance discharges to ground. Thus, the C_{s3} portion of the circuit

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Switched-capacitor filters suit integrator-type circuits

produces no parasitic-capacitance errors.

Finally, you can assign some practical values to the SC-filter circuit shown in **Fig 9.** Assume that you want this bandpass filter to exhibit a 1-kHz peaking frequency and a Q of 20. Assuming a 20-pF feedback capacitance for each op amp, $C_{s1}=C_{s3}=5$ pF, while $C_{s2}=0.25$ pF. These values indicate the relationship between capacitance-value spread and Q, for the previously derived expression for C_{s2} shows that the ratio of C_{s2} to C is inversely proportional to Q.

State-variable filters offer many advantages, but for high-Q circuits, they can become very sensitive to their components' values—unless they operate at an extremely high sampling rate. Unfortunately, though, op-amp integrators' settling times and slew-rate limitations restrict sampling rates.

However, one way to achieve low component-value sensitivities at moderate sample rates is to utilize leapfrog filters—active implementations of classical LC ladders synthesized with both load and source terminations. Because such filters exhibit low sensitivity to their inductor and capacitor values in the passband, they amply suit SC-filter techniques.

As an illustration of the leapfrog-filter design process, consider **Fig 10**'s fifth-order Chebyshev low-pass filter, whose parameter values set ripple at 0.1 dB and normalize the cutoff frequency to 1 radian/sec. The following equations apply to this circuit:

$$I_0 = \frac{V_1 - V_0}{L_0 s} \qquad V_1 = \frac{I_1 - I_0}{C_1 s} \qquad I_1 = \frac{V_2 - V_1}{L_1 s}$$

$$V_2 = \frac{I_2 - I_1}{C_2 s} \qquad I_2 = \frac{V_3 - V_2}{L_2 s} \qquad V_3 = V_i - I_2 R_s.$$

Note that the only operations indicated by these equations are differential integrations, multiplications by constants and algebraic summations. The operational diagram shown in **Fig 11** can thus embody these same functions in its leapfrog arrangement. To implement all of **Fig 11**'s integrators with op amps, the current nodes shown along the diagram's bottom must be transformed into voltage nodes by multiplying them by an arbitrary scaling resistance R_0, and the integrators' gains must be modified (**Fig 12**).

In this example, $R_s=R_L=1\Omega$, but in any case, the scaling resistance R_0 normalizes both of these values. The differential integrators now suit implementation in SC form as shown in **Fig 13.**

Note that **Fig 13**'s primed capacitors implement inductors; from the normalizations indicated in **Fig 12,** $L/R_0=R_0C'$ or $C'=L/R_0^2$.

This relationship hinges on the fact that the inductance-simulating integrator's gain (or time constant) determined by C′ must be the same whether you express the inductor's transfer function in terms of inductive impedance or RC/op-amp voltage gain. In this example, $R_0=1\Omega$, so $C'=L$.

Working in conjunction with the feedback capacitors shown in **Fig 13,** a constant, α, sets integrator gain. For an inductance simulator, the following expression results:

$$\frac{1}{Ls} = \frac{1}{R_{eq}C's} = \frac{1}{\frac{1}{f_s}\frac{C'}{\alpha' C'}s} = \frac{\alpha' f_s}{s}.$$

Thus, $\alpha'=1/Lf_s$. Similarly, for a capacitance simulator, the result is $\alpha=1/Cf_s$.

Additionally, if you want to scale the filter's frequency response so that it cuts off at f_0 rather than

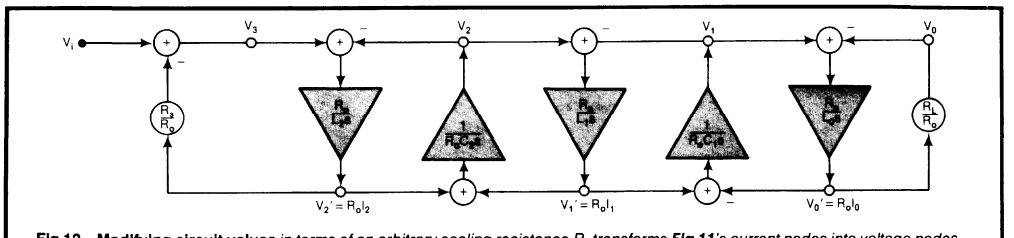

Fig 12—Modifying circuit values *in terms of an arbitrary scaling resistance R_0 transforms* **Fig 11***'s current nodes into voltage nodes.*

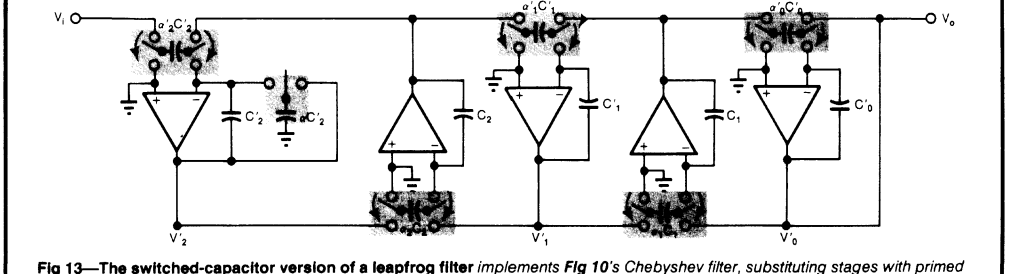

Fig 13—The switched-capacitor version of a leapfrog filter *implements* **Fig 10***'s Chebyshev filter, substituting stages with primed capacitors for inductors. (Arrows on switches indicate the alternating-phase relationship between adjacent stages.)*

2π, $s/2\pi f_0$ must replace s. And because inductive impedance equals Ls, $L/2\pi f_0$ must replace all inductor values, and $C/2\pi f_0$ all capacitor values. Combining this frequency scaling with the values for α and α' (for an assumed 1-kHz cutoff and a 25-kHz sampling rate) furnishes the following final values:

$$\alpha_0' = \frac{1}{\frac{L_0}{2\pi f_0} f_s} = \frac{2\pi f_0}{L_0 f_s} = \frac{2\pi \times 10^3}{1.1468 \times 25 \times 10^3} = 0.219$$

$$\alpha_1 = \frac{1}{\frac{C_1}{2\pi f_0} f_s} = \frac{2\pi f_0}{C_1 f_s} = \frac{2\pi \times 10^3}{1.3712 \times 25 \times 10^3} = 0.183$$

$$\alpha_1' = \frac{2\pi \times 10^3}{1.9750 \times 25 \times 10^3} = 0.127$$

$$\alpha_2 = \frac{2\pi \times 10^3}{1.3712 \times 25 \times 10^3} = 0.183$$

$$\alpha_2' = \frac{2\pi \times 10^3}{1.1468 \times 25 \times 10^3} = 0.219.$$

Leapfrog-ladder SC filters are currently employed in a wide variety of products, such as Intel's 2920 PCM filter, Silicon Systems' DTMF telephone chip and Reticon's R5604/R5605/R5606 16-pin-DIP bandpass filters.

To prevent excess phase lag, which can enhance the filter's Q, the switch phasing in **Fig 13**'s circuit alternates between adjacent integrators. This procedure decreases excess phase by creating a ½-period phase lead in one integrator, followed by a ½-period phase lag in the next one. **EDN**

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3. Hosticka, B J; Broderson, R W; and Gray, P R; "MOS Sampled-Data Recursive Filters Using Switched-Capacitor Integrators," *IEEE Journal of Solid State Circuits*, Vol SC-12, No 6, December 1977, pgs 600-608.

Author's biography

A M Davis is an associate professor at San Jose State University, CA, where he teaches electronics and circuit theory. He also teaches at the University of Santa Clara, CA, and has worked at Bell Labs and Eastman Kodak Research Lab, in addition to doing consulting work at several other firms. Professor Davis' leisure-time activities include backpacking, ham radio, reading, freelance writing and music.

SESSION XII: DATA COMMUNICATION ICs

THAM 12.3: Monolithic Filters for 1200 Baud Modems

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EG&G Reticon
Sunnyvale, CA

Les Querry
Penril Corp.
Rockville, MD

WITH THE RAPID evolution of the computer industry, demands for data communication through voice channels have greatly increased, calling for higher speed modems (modulator and demodulator units). A significant portion of the cost for a high-speed modem system comes from the filter circuits because of their stringent requirements. Until now, they have been manufactured either with hybrid devices using lengthy and costly trimming process, or with bulky discrete active filters with precision components. With the advent of switched-capacitor filter techniques, MOS technology presents an optimum approach in terms of cost, size, accuracy and reproducibility. Two chips of monolithic filters designed to replace the conventional hybrid filters in a 1200-baud full-duplex modem have been fabricated using this switched-capacitor filter technology. The design and the performance of the filters will be described.

The implementation of the two bandpass filters is based on characteristics set earlier*. The filters, each containing ten cascaded second-order biquads, are centered around 1200Hz and 2400Hz. An important characteristic of the filter is the amount of interband rejection which attenuates the local transmit carriers in the modem. Another critical requirement of these filters is the phase linearity across the passband to assure equal delay of all frequency components passing through the filters. Three second-order elliptical rejection filters and two low- (or high-) pass filters were designed to achieve the frequency response of the higher (or lower) bandpass filter, while the remaining five sections have allpass characteristics which equalize the delay response.

The basic building block of the generalized biquad section is shown in Figure 1. Note that there are three input paths to the biquad. Various combinations of these paths will achieve allpass, bandreject, highpass, lowpass, and bandpass functions[1]. With proper phasing of the switches, the biquad can realize the general second-order transfer function including the right-half-plane zeros of the allpass section. The linear-phase characteristics of the modem filters are best preserved by using the matched z transform when the switched-capacitor version of the continuous prototype is constructed[2]. The mapping of poles and zeroes from the s domain into the z domain is performed by simply substituting $(1\text{-}z^{-1}e^{-aT})$ for (s+a). The accuracy of this approximation is of course limited by the sampling frequency chosen. The z transfer function of the circuit shown in Figure 1 is

$$H(z) = \left(\frac{C_6}{C_4+C_8}\right)\frac{z^2 - \left(2+\frac{C_5}{C_6} - \frac{C_1}{C_2}\frac{C_3}{C_6}\right)z + \left(1+\frac{C_5}{C_6}\right)}{z^2 - \left(2+\frac{C_8}{C_4} - \frac{C_7}{C_2}\frac{C_3}{C_4}\right)\left(\frac{C_4}{C_4+C_8}\right)z + \left(1-\frac{C_8}{C_4+C_8}\right)}$$

The simulation results of the amplitude and phase response with the matched z transform showed that, for a sampling rate to signal frequency ratio of 30, the deviation of the amplitude from the continuous prototype is much less than 0.01dB and that of phase is less than 0.2°, for moderate Q, over a frequency range of 1000Hz.

Double-poly NMOS technology offers good-quality poly-to-poly capacitors. High accuracy in capacitor ratios is achieved with edge-controlled and metal-interconnected capacitor arrays. A 200mil^2 operational amplifier of 2000 open loop gain is used on this chip. A TTL clock of 1.2288MHz required to trigger the digital circuitry on the chip to provide clock timing for the filters.

A photomicrograph of the lower-band filters is shown in Figure 2. The relatively large areas dedicated to the capacitors are dictated by the high accuracy needed for the phase response. Figure 3 shows the experimental frequency response of the two bandpass filters. The slight peaking near the edge of the high band was designed to compensate for the average phone-line droop. The frequency-dependent delay response, which is a critical requirement for low bit-error-rate operation, is also shown in Figures 4 and 5. Both chips achieve more than the 50dB dynamic range required for most of the modem applications. An interband rejection of more than 55dB is obtained. With a ±10V power supply, the chip dissipates less than 250mW. The uniform chip-to-chip frequency and delay characteristics (achieved without trimming) and the high temperature stability result in excellent modem performance which provides low bit-error rates even at low signal levels under worst-case line conditions.

Acknowledgments

The authors would like to thank G. P. Weckler and R. W. Brodersen for their direction and helpful advice.

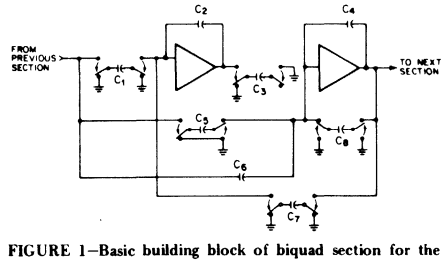

FIGURE 1—Basic building block of biquad section for the filter.

*Bell 212 filters

[1] Cox, D.B., Lin, L.T., Florek, R.S., and Tseng, H.F., "A Real-Time Programmable Switched Capacitor Filter", *IEEE Journal of Solid-State Circuits*, p. 972-977; Dec., 1980.

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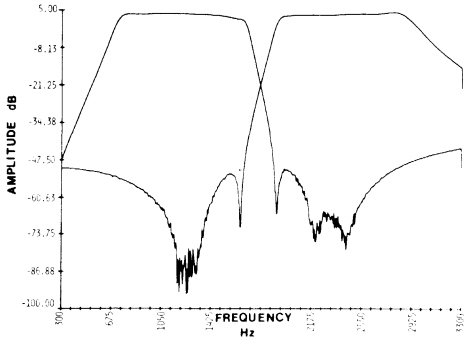

FIGURE 3—Frequency response of the bandpass filters for the modem.

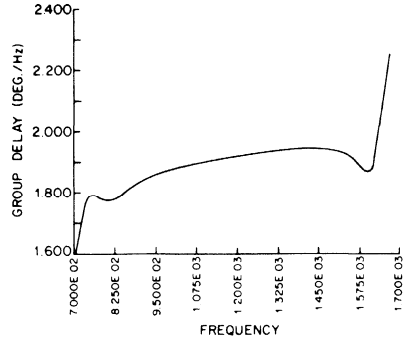

FIGURE 4—Typical delay response vs frequency of the lower band filter.

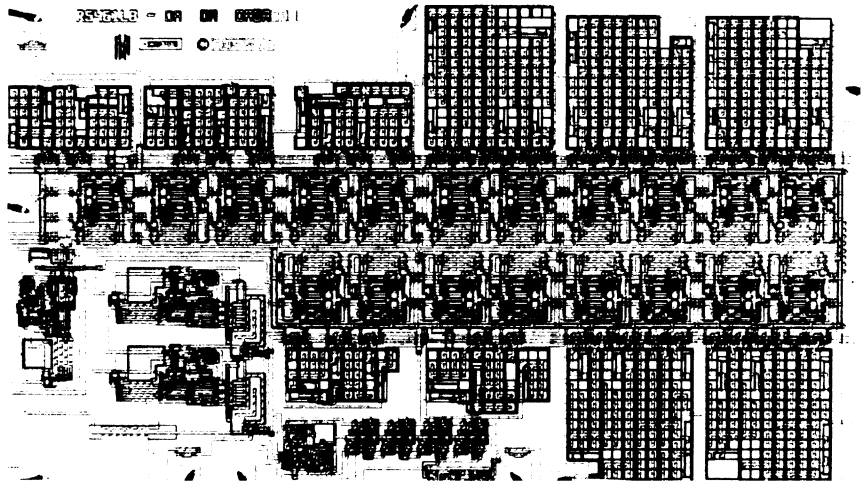

FIGURE 2—Photomicrograph of modem lower-band filter chip.

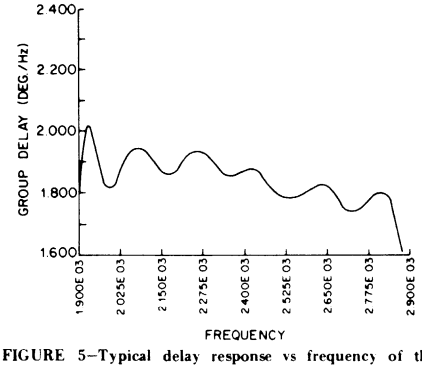

FIGURE 5—Typical delay response vs frequency of the higher band filter.

SESSION XIX: SPEECH PROCESSING

FAM 19.5: A Monolithic Audio Spectrum Analyzer for Speech Recognition Systems

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THE RAPID DEVELOPMENT OF MOS IC technology has been utilized in many areas of man-machine interface applications. A monolithic audio spectrum analyzer, designed to perform the spectrum-analysis function of a speech recognition system, has been implemented with double-poly NMOS technology. The chip was designed using switched-capacitor filter techniques. It contains one hundred operational amplifiers and measures 225 x 280mils.

A functional block diagram of the analyzer section of a typical speech-recognition system is shown in Figure 1. After the voice signal is frequency emphasized and level adjusted, it is applied to the spectrum-analyzer chip. The outputs of the chip represent the corresponding amplitudes of the frequency components of the incoming voice signal over sixteen pre-defined bands of a filter bank. The amplitude outputs can then be externally digitized, encoded, compressed and compared with a set of reference data. A variety of algorithms can be used to determine the similarity to these data, thus achieving recognition.

A functional block daigram of the chip is shown in Figure 2. The extraction of amplitudes corresponding to each channel are accomplished by passing the signal through sixteen parallel channels; each contains a second-order Butterworth bandpass filter (BPF), a precision half-wave rectifier, and a second-order Butterworth low-pass filter (LPF). The detailed schematic for a single channel is shown in Figure 3. Both bandpass and low-pass filter functions are implemented with switched-capacitor filters in a state-variable configuration. The center frequencies and the bandwidths of the BPFs designed to cover the voice band are shown in Table 1. The cutoff frequency of the low-pass filters was designed to be 25Hz. Effective termination of the BPF was realized with a capacitive feedback scheme to optimize the overall capacitor ratios and dynamic range. The Z-domain transfer function for the bandpass filter and low-pass filter are

$$H_{B.P.}(Z) = \frac{-\alpha_3 \alpha_1 (Z-1)}{Z^2 - (2-\alpha_1\alpha_2-\alpha_1^2) Z + (1-\alpha_1\alpha_2)}$$

$$H_{L.P.}(Z) = \frac{-\alpha_3 \alpha_1 Z}{(1+\alpha_2) Z^2 - (2+\alpha_2-\alpha_1^2) Z + 1}$$

where α_1, α_2 are modified from the continuous-time value to compensate for the delay effect[1]. A precision half-wave rectifier utilizing diodes and resistors was used with two MOS transistors to implement the diode function as shown in Figure 3. The diode-connected transistor between the inverting input and output of the operational amplifier provided a feedback path during the inactive cycle. It prevented the output from going into a saturation state, hence relaxed the slew-rate requirement of the operational amplifier[2]. Gain of the rectifier during the active cycle was determined by a closely matched polysilicon resistor ratio. The voltage difference between the offset of the bandpass filter and the reference voltage of the rectifier has been a major concern as a limiting factor for the system dynamic range. Therefore, a dc blocking capacitor was employed to reduce the offset of the bandpass filter and a dummy channel was used to generate a reference voltage for the rectifier to enhance further the small signal rectification. The two integrators of the LPFs were sampled at 31.25kHz and 15.625kHz. The higher sampling rate for the first stage was required to prevent higher-order harmonic components of the rectified waveform from aliasing into the LPF and the lower sampling rate for the second stage was to reduce the capacitor ratios. Since the requirements on the operational amplifier for the low-pass is not as stringent, a simple differential-pair operational amplifier with a gain of 40 was used for the integrator to save power and area[3].

The outputs of 16 LPFs are multiplexed through sample-and-hold circuitry controlled by internally generated timing and four

fo (Hz)	*Bandwidth (Hz)*	*Approximate Band Coverage*	
		f l	*f* h
260	130	203	333
390	130	330	460
520	130	459	589
650	130	588	718
780	130	718	848
910	140	843	983
1060	160	983	1143
1220	180	1133	1313
1400	200	1303	1503
1600	220	1494	1713
1820	250	1699	1949
2070	300	1925	2225
2370	340	2206	2546
3035	1030	2563	3593
4272	1445	3610	5055
5997	2005	5077	7083

Table 1—Filter characteristics.

[1] Cox, D.B., Lin, L.T., Florek, R.S., and Tseng, H.F., "A Real-Time Programmable Switched-Capacitor Filter", *IEEE J. Solid-State Circuits*, p. 972-977; Dec., 1980.

[2] Gray, P.R., and Meyer, R.G., "Analysis and Design of Analog Integrated Circuits", *John Wiley & Sons*, p. 555-561; 1977.

[3] Hosticka, B.J., Brodersen, R.W., and Gray, P.R., "MOS Sampled Data Recursive Filters Using Switched Capacitor Integrators", *IEEE J. Solid-State Circuits*, p. 600-608; Dec., 1977.

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input address lines. These LPF outputs are also simultaneously accessible externally. A 1MHz TTL clock is required to trigger the internal logic that provides all of the necessary timing.

The device was designed to operate with a ±10V power supply. Dynamic range is limited by the non-uniformity of the offsets at the inputs of the rectifiers across the channel bank. With the close matching of the layout, more than 43dB of system dynamic range has been obtained, while an input signal as small as 15mV p-p was detected. The transfer function of each channel shows a linearity of better than 1%. Center frequencies of the filters are typically within 1% of the design values. The chip draws about 35mA.

Acknowledgments

The authors would like to thank G. P. Weckler and R. W. Brodersen for their support and helpful discussion.

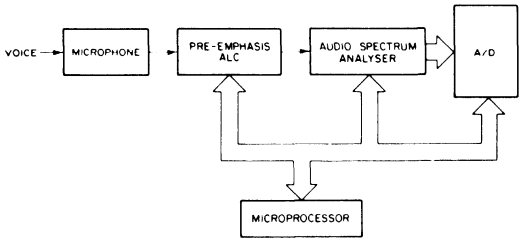


FIGURE 1—Functional block diagram of analyzer section of speech recognition system.

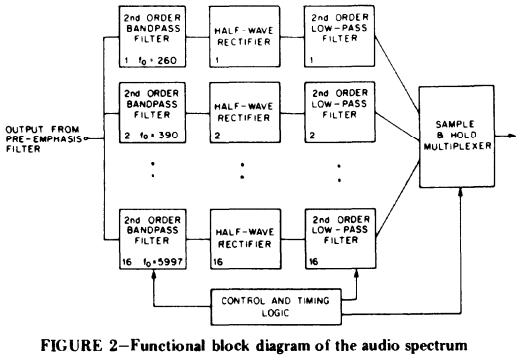


FIGURE 2—Functional block diagram of the audio spectrum analyzer chip.

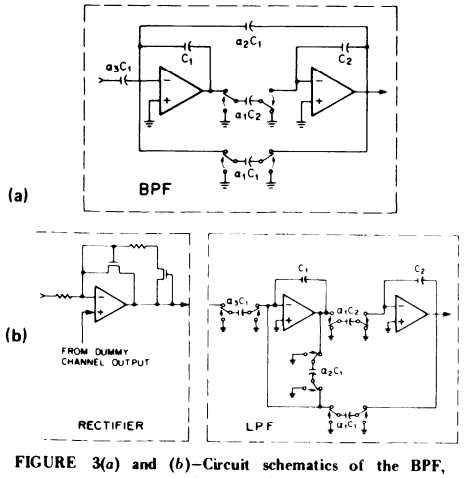
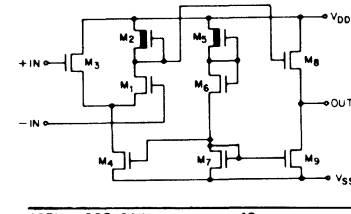


FIGURE 3(*a*) and (*b*)—Circuit schematics of the BPF, rectifier and LPF.



OPEN LOOP GAIN	40	(b)
OFFSET	15mV	
OUTPUT VOLTAGE SWING	+6.8V, −4.1V WITH 30pF LOAD	
UNITY GAIN FREQUENCY	2.5MHz	
SLEW RATE	+3V/μs, −1.0V/μs WITH 30pF LOAD	
CMRR	+42dB	
PSR	−50dB, −35dB FOR V_{DD} AND V_{SS}	

FIGURE 4(*a*) and (*b*)—Schematic and performance summary of differential pair amplifier.

A LOW SPEED SWITCHED CAPACITOR MODEM FILTER I.C. THAT IS COMPATIBLE WITH THE C.C.I.T.T. V.21 MODEM

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ABSTRACT:

An integrated circuit is described that performs all the filtering functions of a low speed 300 baud full duplex modem and is compatible with the C.C.I.T.T. V.21 standards. The chip is fabricated in a double-polysilicon NMOS process and contains a clock oscillator, input gain control, and answer/originate multiplexing capability, output limiter for the receive channel, clock filters, and two ten pole bandsplit filters. The bandsplit filters are specifically designed to compensate for both amplitude and phase distortions.

INTRODUCTION:

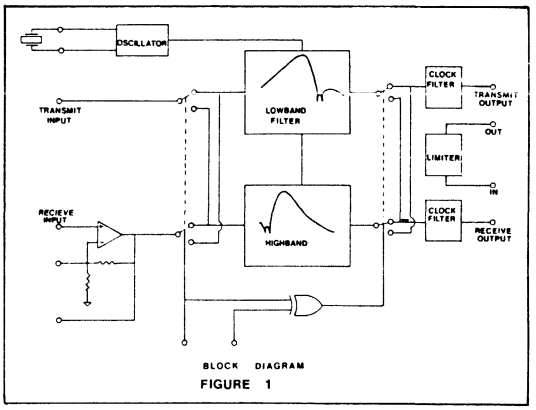
The most convenient way to transmit low speed digital data is to adapt the many existing telephone facilities for data transmission. However, transmission facilities designed to handle voice traffic have characteristics which make it difficult to directly transmit digital data. Unfortunately, phone lines have a bandwidth of only 300Hz to 3300Hz (about 3KHz), which is limiting with respect to data transmission speeds and characteristics. To overcome this bandwidth limitation, the digital data are first encoded into an audio frequency signal, then the encoded signal is transmitted over the audio transmission channel. The device which performs this conversion is called a modem. Modem is an acronym for Modulator/Demodulator. A modem connects to a digital device such as a computer terminal, and by modulating a carrier signal, converts transmission to a remote terminal or computer. A modem also accepts incoming analog signals from the transmission line and decodes them into digital form for the digital device.

A simple and low cost modulation scheme employed in low speed modems is frequency shift keying (FSK). FSK uses two discrete frequencies, one is called "mark" and the other is called "space." In Europe and Japan the higher frequency (space) is designated as an 0 bit and the lower frequency (mark) is designated as 1 bit.

A popular modem in use today for low speed full duplex applications in Europe and Japan is the C.C.I.T.T. V.21 modem. Such a modem requires bandsplit filters to separate the two FSK data channels. Typically, these filters are constructed using thick film hybrid technology or bulky discrete components. These can be expensive, require large areas of board space and often need trimming. The advent of distributed computing has brought about an increasing need for low cost, more compact data communications. State of the art switched capacitor filters employing MOS/VLSI technology are an ideal way to achieve these results. This paper describes an integrated circuit that has been designed to meet this need and the circuit techniques employed to realize these filters.

FILTER DESIGN:

A 300 baud bandsplit switched capacitor modem filter chip has been fabricated in a double poly NMOS process. A System Block Diagram is shown in Figure 1. The transmit and receive channels for the C.C.I.T.T. V.21 modem are centered at 1080Hz and 1750Hz, respectively. The channel frequency assignment is shown in Table I. For both transmission and reception, it is necessary to reject signals that may be present in the adjacent channel. Interference which has several sources must be filtered out.



BLOCK DIAGRAM

FIGURE 1

C.C.I.T.T. V.21 MODEM CHANNEL ASSIGNMENTS

MODE		TRANSMIT FREQUENCY	RECEIVE FREQUENCY
ORIGINATE:	MARK	980Hz	1650Hz
	SPACE	1180Hz	1850Hz
ANSWER:	MARK	1650Hz	980Hz
	SPACE	1850Hz	1180Hz

TABLE I

The transmit filter has primarily three functions to perform. The first is to reject the out-of-band harmonics generated by the

transmit carrier and the second is to attenuate spurious signalling harmonics above 4KHz in conformance with the European PTT requirements. The last function is to control relative transmit carrier level. The receive filter is the most dominant section to the overall performance of the modem. It determines the modem's dynamic range and data error performance on low signals to noise ratio telephone connections. To achieve these results, two tenpole bandpass filters are realized by cascading five second order sections. The lowband has three bandpass sections and two lowpass notch sections while the highband has three bandpass sections and two highpass notch sections cascaded as shown in Figure 2. The basic building block of the generalized biquad section used in implementing these filters is shown in Figure 3.

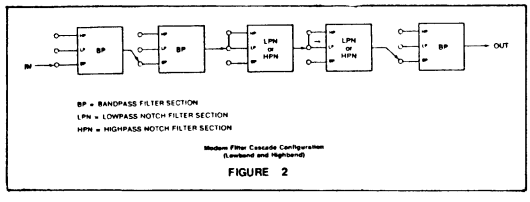


FIGURE 2

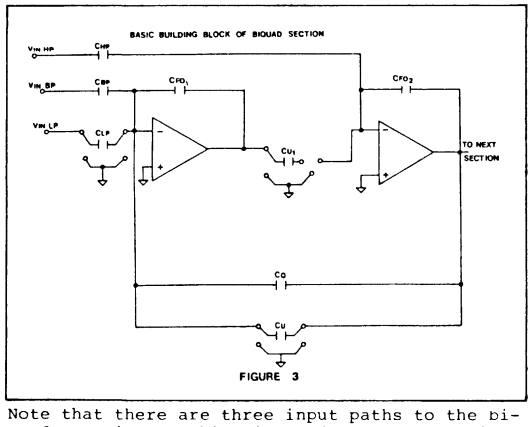


FIGURE 3

Note that there are three input paths to the biquad. Various combinations of these paths will achieve the required bandpass, lowpass and highpass notch sections. The generalized Laplace transform transfer function of the biquad section, ignoring the delay effect, is:

$$\frac{Vo}{Vi}(s) = H(s) = \frac{C_{HP}}{C_{FO2}} \left[\frac{s^2 + \frac{C_{BP}\,C_U\,F_C}{C_{FO1}\,C_{HP}}\,s + \frac{C_{LP}\,C_U\,F_C^2}{C_{FO1}\,C_{HP}}}{s^2 + \frac{C_Q\,C_U\,F_C}{C_{FO1}\,C_{FO2}}\,s + \frac{C_U\,C_{U1}\,F_C^2}{C_{FO1}\,C_{FO2}}} \right]$$

If the above transfer function is compared to the generalized second order biquad function:

$$H(s) = G \left[\frac{s^2 + \frac{2\pi F_z}{Q_z}\,s + (2\pi F_z)^2}{s^2 + \frac{2\pi F_p}{Q_p}\,s + (2\pi F_p)^2} \right]$$

It is then easy to solve for Fp, Fz and Qp:

$$F_p = \frac{C_U \times F_C}{2\pi \times C_{FO2}} \qquad (1)$$

$$Q_p = \frac{C_{FO1}}{C_Q} \qquad (2)$$

and by rearranging:

$$F_z^2 = \frac{F_p^2 \times C_{LP} \times C_{FO2}}{C_U \times C_{HP}} \qquad (3)$$

Similarly, the lowpass, highpass and bandpass gains are obtained as follows:

$$\text{Lowpass Gain} = CLP/Cu \qquad (4)$$

$$\text{Highpass Gain} = CHP/C_{FO2} \qquad (5)$$

$$\text{Bandpass Gain} = \frac{C_{BP} \times QP}{C_{FO1}} \qquad (6)$$

Where fc is the sample rate at which the switching capacitors are switched and for the filter design Fc = 250KHz.

Since the generalized biquad transfer function does not take into consideration the sampled data effects on the filter, it is necessary to take them into account to determine the exact capacitor values. Due to the sample rate to center frequency ratio (fc/fo) being at least 20 to 1, these effects are small but still significant. The correct transfer function can be obtained by simply substituting $(1-z^{-1}e^{-at})$ for (s+a) in the generalized biquad transfer function.

The Q values used in designing these filters vary from 1 to 6 depending on the filter type. Low Q's were used in order to maintain low group delay distortion, a very critical parameter in modems. One of the main advantages of this design is the fact that the poles and zeros of the transfer function can be determined by the ratios of capacitors, thus assuming high accuracy since capacitor ratios can be controlled to better than 0.5% depending on the unit capacitance size used.

FILTER DESIGN PARAMETERS:

Generally, modem filters must provide sufficient adjacent channel rejection in order to provide good bit error performance. Typically, the channel rejection for these filters should be better than 45db. The minimum bandwidth required in FSK modems is usually determined according to the modem's data rate. In such systems data transmission is recovered by detecting the center of the transmit/receive channels and their respective first sidebands. A modem operating at a data rate of 300 bits per second or 300 baud should have the first sideband occuring at ±150Hz from the center of the channels. For the C.C.I.T.T. V.21 modem, they occur at 1080 ±150Hz, and 1750 ±150Hz. Therefore, a 300 baud modem should be able to encode and decode a 150Hz square wave input into mark and space frequencies. Hence a minimum bandwidth of 300Hz is required in the filters. The amount of passband ripple in 300 baud modems is not a critical parameter, since the output of the receive filter is usually fed into an amplitude limiter. However, a critical parameter of these filters is the phase linearity over the 300Hz bandwidth. All frequency components that pass through the filters must be equally delayed in time or smearing of the data occurs. This phase distortion is known as inter-symbol or inter-bit interference.

Typically, frequencies within the filter's 300Hz bandwidth should not undergo greater than 1 millisecond variation in group delay including filters, phone line and all other delay sources.

Usually to achieve linear phase characteristics in the passband delay equalizer filters are used. But the design goal of these filters, in addition to rejecting out of band signals, is to achieve linear phase characteristics without the need for delay equalizers. This was done primarily by using low Q values ranging from 1 to 6 for designing the filters. The relationship between group delay and phase is given in the equation:

$$Td = \frac{\triangle \phi}{\triangle f} \times \frac{1}{360°/\text{cycle}}$$

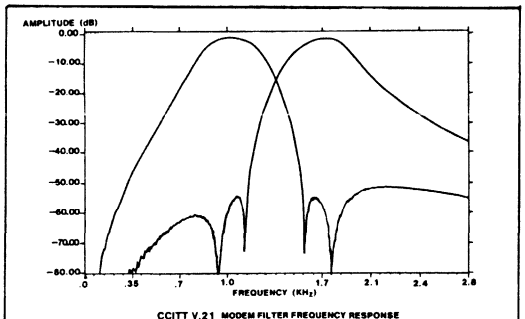
Where: $\triangle \phi$ = change of phase in degrees

$\triangle f$ = change of frequency in Hz

The group delay of the transmit and receive filters is very important. Group delay relates to the propagation time difference for a mark frequency to pass through the filter as compared with a space frequency. Group delay time should be kept small as compared with the modem's baud rate to lessen the effects of distortion and bias jitter.

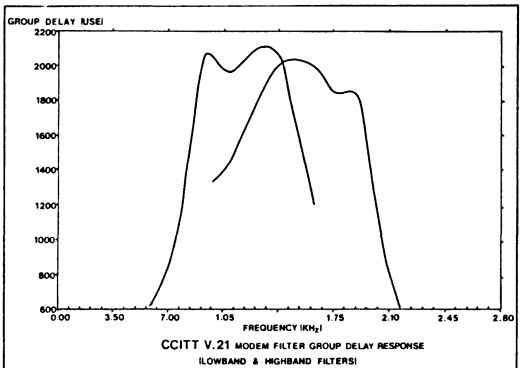
ELECTRICAL PERFORMANCE:

The measured amplitude and group delay response plots of the modem filters are shown in Figures 4a and 4b. The modem filters output noise spectrum plots are shown in Figures 5a and 5b. The measured performance parameters for the chip are listed in Table II.



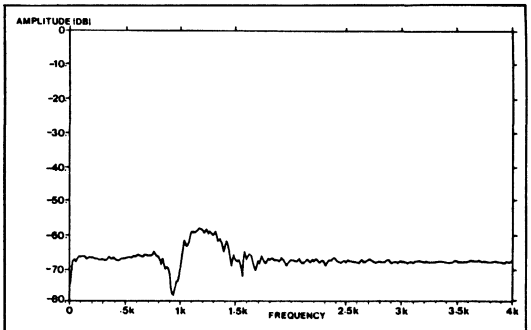
CCITT V.21 MODEM FILTER FREQUENCY RESPONSE (LOWBAND AND HIGHBAND FILTERS)

FIGURE 4a



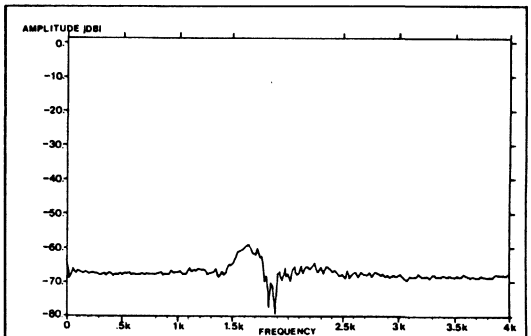
CCITT V.21 MODEM FILTER GROUP DELAY RESPONSE (LOWBAND & HIGHBAND FILTERS)

FIGURE 4b



CCITT V.21 LOWBAND FILTER OUTPUT NOISE SPECTRUM

FIGURE 5a



CCITT V.21 HIGHBAND FILTER OUTPUT NOISE SPECTRUM

FIGURE 5b

MEASURED PERFORMANCE PARAMETERS FOR MODEM FILTER

Adjacent Channel Rejection	53dB
3db Bandwidth	350Hz
Group Delay Variation (in 300Hz Passband)	200μs
Passband Ripple	1dB
Power Supply Range	±4v to ±10v
Operating Current	12mA
Dynamic Range	80dB
Crosstalk	-62dB
Distortion (THD)	≤.5%
Output Noise	>60dB
Maximum Signal	12Vp-p
Output Voltage Swing	12Vp-p
Maximum Power Dissipation	240mW

WHEN USED IN A MODEM CIRCUIT THE FOLLOWING RESULTS WERE OBTAINED:

ERROR RATE LESS THAN ONE ERROR IN 10^5 BITS AT 6dB SIGNAL TO NOISE RATIO; FLAT NOISE FROM 0 TO 4KHz.

TABLE II

The measured amplitude and phase response of the filters showed that for a sampling rate to center frequency ratio (fc/fo) of 50, the deviation of the amplitude from the simulation results using Z-transform is much less than .5db and that of phase is less than .5° for Q values less than 6 over a frequency range of 1000Hz. Double-poly NMOS technology offers good quality poly-to-poly capacitors. High accuracy in capacitor ratios is achieved with

metal-interconnected capacitor arrays.

Other features on the chip include a receive channel input which has an adjustable gain stage. The gain stage may be varied from 0db to 20db using an external resistor between the two receive gain control pins. Gains of 0db or 20db may be selected by shorting or opening the two pins. An operational amplifier limiter is available for use on the output of the receive channel. It has a gain of 1000 and a typical offset of less than 15mv. It may be used as a buffer between the receive output and a demodulator circuit. Both transmit and receive output paths have a continuous time second order Salen and Key type lowpass anti-clock filters to reduce clock feedthrough. Typical feedthrough at the sample rate is less than 5mv. An on chip multiplexer is also included which switches the low-band and highband filters between channels, depending on whether the modem is in the answer or originate mode. The mode selection is determined by an external pin. The multiplexer also has a self test pin which switches the same filter to transmit in and receive out. The chip is designed to operate with a master clock of 1MHz which may be supplied by an external CMOS or TTL clock or an on-chip oscillator which uses an external crystal. A 200 mil^2 operational amplifier is used in the filters and the chip contains a total of 24 operational amplifiers. The Op Amp Circuit Schematic is shown in Figure 6. The chip size is 120 x 180 mil^2 and a chip photo micrograph is shown in Figure 7.

CONCLUSION:

A switched capacitor integrated circuit that performs all the filtering functions for 300 baud modem applications in Europe and Japan is now available. The result of this effort combines high performance, low cost, and ease of use into a single 16-pin package.

ACKNOWLEDGEMENT:

The authors would like to thank Dr. Gene Weckler and Dr. Hsin-Fu Tseng for their encouragement and support, and Ms. Lily Saunders for her mask design effort.

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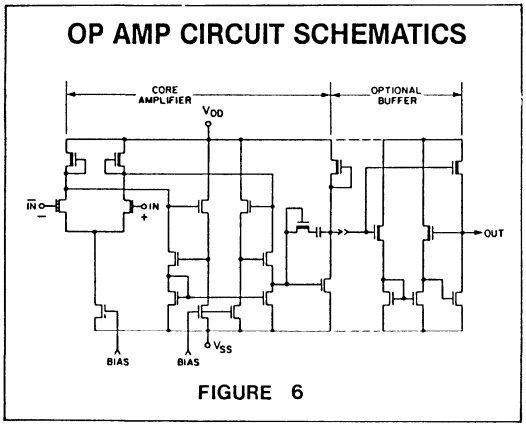

FIGURE 6

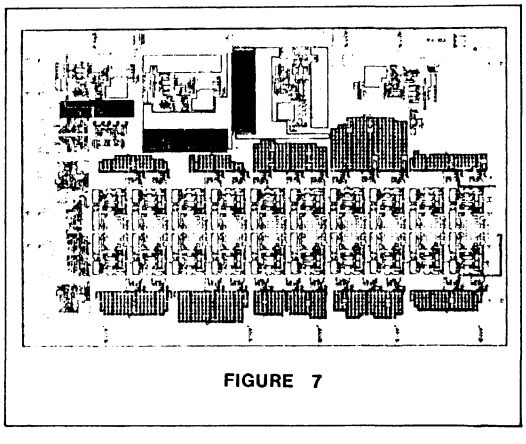

FIGURE 7

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A MASK PROGRAMMABLE SCF AND LOGIC ARRAY FOR SEMI CUSTOM ANALOG SYSTEM INTEGRATION

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Abstract

A metal mask programmable switched capacitor filter and digital logic array chip has been developed to integrate subsystems consisting of filtering and other signal processing functions. A computer-generated metal mask is used to customize prefabricated wafers. This chip was fabricated with a double-poly NMOS process and was designed to provide the same level of high performance and much of the flexibility of a full custom chip while providing the advantages of semi-custom design, i.e., low cost, fast turnaround and proprietary design. This paper describes the techniques used to maximize dynamic range and to maintain excellent capacitor matching accuracy while achieving a high degree of versatility. Design automation tools which were developed to minimize turnaround time are also discussed.

Introduction

Analog LSI circuits based on the switched capacitor technology have been gaining in popularity and importance recently. In many signal processing system applications (e.g., modem, sonar, speech, etc.) complex filtering, modulation/demodulation and other analog signal processing are required. The use of conventional analog building blocks (e.g., bipolar circuits, discrete as well as hybrid RC active components) proved to be bulky and often require either expensive trimming or costly precision components. Custom as well as off-the-shelf switched capacitor circuits have made the implementation of these analog subsystems more economical. Many times the switched capacitor approach turns out to be the only feasible or practical solution. This paper describes a semi-custom chip developed for integrating and reducing the parts counts of analog signal processing subsystems. It is intended to provide the analog system designer an alternative solution to either full custom or standard components. This chip contains 14 metal programmable biquadratic SCF sections and 20 digital array cells. A photograph of the chip layout is shown in Figure 1. Complex mixed analog and digital subsystems can be customized and integrated by a single metal mask. Design automation tools were developed specifically to aid the implementation of the switched capacitor filters (SCFs) and the customization of the metal mask. As a result, turnaround time was minimized and design accuracy was assured. By using novel SCF layout and capacitor construction techniques, complete flexibility and freedom in filter design is achieved while performance is not sacrificed. The applications for this mask programmable SCF and logic array are very extensive. Examples include: high order state variable or classical filters, precision delay equalizers, Hilbert transform filters, modem filters, tracking filters, single chip spectrum analyzer, modulators/demodulators, limiters and zero crossing detectors.

To illustrate this new semi-custom design approach, modem filters for 202/V.23 applications and associated mod/demod circuits were implemented on this chip and the results will be discussed.

Chip Organization and Major Features

A 25 volt NMOS process which has been optimized for both analog and digital applications was chosen because of its low noise performance and lack of latch up. The major circuits on this chip are:

1. 14 Second order sections (28 op amps and associated switches and capacitor arrays. Op amps can be used as "uncommitted" op amps)
2. 2 First order sections (2 op amps and 8 capacitor arrays)
3. 1 Uncommitted op amp
4. 20 Digital gates
5. 8 ÷ 2 flip/flops
6. 2 Two-phase clock generators
7. 1 Crystal oscillator circuit
8. 6 Digital I/O buffers
9. 40 Pads

The heart of the device is the 14 second order sections and the 20 AND-OR-INVERT array cells. Each second order section consists of two low noise and low power op amps, NMOS switches and 9 double poly capacitor arrays. Each op amp. has an open loop gain of 66 dB and bandwidth of 2 MHz. An optional output buffer is available for each of the op amps. Each second order section can be

*No longer associated with EG&G Reticon

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used to implement all first and second order transfer functions. The filter array can also be programmed to obtain ladder filters. The chip operates from a supply range of +/- 3.5 volts to +/- 12 volts at a power consumption of typically 0.25 mA/pole. The switched capacitor filters have a frequency range of 0.05 Hz to over 30KHz. Dynamic range is from 70 to 85 dB, depending on filter complexity. The pole/zero and Q-factor accuracy is better than 1%. Passband accuracy is typically 0.2 dB. A wide clock to corner range of 15:1 to 250:1 is available. The digital array can be used for logic operations as well as to perform signal steering and gating. The digital gates operate up to 6 MHz and the internal logic levels are compatible with the analog levels. The uncommited op. amps. together with the uncommitted capacitor arrays, switches, and digital logic, can be used to implement many important signal detection, modulation and demodulation schemes.

Generation of the Semi Custom SCF and Logic Device

The semi-custom device is prefabricated and inventoried after metal deposition. The many arrays of op amps, switched capacitors, digital gates and peripheral circuitry on this chip are programmed by using a customized metal mask. A large development effort went into the design of the prefabricated chip in order to achieve low noise op amps, to maximize the matching of the switched capacitor ratio, to minimize signal and clock coupling, and to achieve a high degree of versatility. Upon receipt of a custom order, the effort concentrates on the design of the metal mask, the final metal pattern definition and device testing. In order to reduce the design time and cost, and to eliminate errors, the creation of the metal mask has been automated.

The sequence of events in customizing the SCF and logic array is illustrated by a flow chart in Figure 2. User inputs should be in the form of filter transfer functions or pole/zero and Q information, block diagrams of other analog functions and digital logic schematics. First, a preliminary design is performed to see whether the desired signal processing functions and the filter parameters can be implemented within the constraints of the circuits on the SCF and logic array device. If compatibility exists, the filter pole/zero and Q information and other design parameters are entered into a microprocessor based computer (a smart terminal) which is linked to a mainframe computer and to a mask design computer. A specially developed computer program is used to determine the capacitor ratios required for SCF implementation and the necessary capacitor and switch hook-up information. A z-domain simulation file is generated at the same time by the mainframe computer to take into account the sampled data effect in the SCF implementation. The desired filtering functions can be breadboarded together with any other signal processing functions by implementing the calculated capacitor ratios in a standard printed circuit board which emulates the filter sections in the I.C. chip. If the simulation results meet the specifications and are confirmed by breadboarding, the circuit design file (including section type, capacitor values and the interconnection information) is sent to the mask design computer. This graphics computer then generates data for the customized portion of the metal layer which, when merged with the pre-defined portion of the metal layer, establishes the final metal mask. The processing of the inventoried SCF and logic array wafers are then completed by defining the metalization pattern using the customized metal mask.

The Biquadratic SCF Building Block

The basic SCF building block on this device is the biquad section shown in Figure 3. Each biquad section consists of two op amps, nine capacitors and associated switches. Each of the capacitors illustrated in Figure 3 actually consists of an array of programmable capacitors. In the uncommited chip, prior to metallization, the op amps, switches and capacitors are unattached. The components within each SCF building block are selected by placing short metal jumpers in a predefined metal bussing grid. This technique easily lends itself to design automation in customizing the metal mask. As mentioned above, a metal connection placement routine is used to program the SCF sections thus avoiding the use of more complex and expensive metal routing techniques.

The biquad implementation illustrated in Figure 3 was chosen for maximum versatility and minimum component count. It can be programmed to implement all useful second and first order transfer functions which can be derived from the following general biquad transfer function:

$$\frac{V_o}{V_1}(S) = H(S) = \frac{G\left(S^2 + \frac{2\pi F_z}{Q_z} S + (2\pi F_z)^2\right)}{S^2 + \frac{2\pi F_p}{Q_p} S + (2\pi F_p)^2}$$

If the desired filter characteristics are specified in terms of magnitude and phase (or group delay) response curves, the pole/zero frequency and Q-factor representation can be obtained by using filter synthesis programs.

The Design and Layout of The Capacitor Arrays

In switched capacitor filters the accuracy of the filter response is determined by the accuracy of capacitor ratios. For maximum flexibility in a programmable filter and to accommodate a large range of ratios of the switching clock frequency to the filter center/corner frequency, a large range of capacitor ratios should be realizable. This creates a logistics problem in the design of a programmable device. On the one hand, the size of the minimum capacitor, the unit capacitor, should be large to optimize performance. On the other hand, to achieve capacitor ratios greater than 100, each capacitor would require more than 100 unit capacitors, leading to an intolerably large chip. This dilemma was solved by using a scaling scheme.

The scaling scheme involves using capacitive divider

networks as illustrated in Figure 4. If ten unit capacitors are used as building blocks, obviously they can be connected in paralell as in Figure 4(a) to represent a total capacitance ranging from 1 to 10 units as seen by the output of the first op amp. Or they can look like an equivalent capacitance ranging from 0.1 to 1/3 of a unit capacitor if they are connected as a T-type network as shown in Figure 4(b).

Each of the 9 capacitors in a section contains more than 20 unit capacitors. To achieve complete design flexibility while at the same time maintaining accuracy, each unit capacitor array can also be connected to an array of non integer capacitors to obtain any arbitrary capacitor ratio (within the maximum ratio limitation of about 250:1) to better than 1% accuracy. Furthermore, by carefully matching the peripheral to area ratio of all capacitors, errors caused by process variations are minimized. A standard deviation of better than 0.1% in the capacitor ratios can be achieved. Thus, typically, the center/corner frequencies and Q-factors can be programmed to better than 1% accuracy.

A typical capacitor array, corresponding to four unit capacitors, is shown in Figure 5, where the shaded rectangles indicate metal jumpers added at the customizing stage. Each unit capacitor consists of two interconnected half-units. The capacitance is formed by the plate capacitance between the first polysilicon layer (large rectangle) and the second polysilicon layer (squares) which are interconnected by metal jumpers. The small second poly rectangles at the outer boundary of the capacitance array serve as etch control to further eliminate variations caused by processing.

Design Automation Techniques for Custom Metal Mask Generation

As discussed before, the preprocessed uncommitted chip contains all the necessary building blocks for a complex signal processing device. To customize the device, the op amps, capacitor arrays, switches, digital circuitry, signal and clock lines have to be interconnected properly via the metal layer. This step, involving the conversion of the filter specifications to the establishment of the connection routing and capacitance ratios, and the subsequent translation of this information into the design of the metal layer, is still a sizeable task. Fortunately this step has been automated thus reducing design time by a large factor, and reducing the possibility of errors.

On the engineer's microprocessor based computer terminal, the section types, interconnection scheme and capacitor ratios are determined. After verifying that the resulting design meets the desired filter specifications using z-transform simulation on a mainframe computer, the design file is transferred to the layout design computer where the custom metal mask is laid out. Basically the data is transferred from the computer terminal in a special sequence. Section by section the capacitance values for each of the 9 capacitors are transferred and the section type is indicated. Additional information, for example clock phasing, buffer options, digital circuit hookup are transmitted, and the layout design computer takes over. Depending on the size of the capacitor, it decides whether or not scaling is required to assure that the capacitor can be accommodated within the predetermined constraints. The computer then places the appropriate metal jumpers in a predefined metal bussing grid to generate the capacitor scaling networks and to select all the necessary capacitor building blocks. After the 9 capacitors for a section have been designed, they are transferred to a section layout cell. In each section layout cell additional jumpers are placed to connect the capacitors with the switches and op amps. Then all section cells are transferred to the final mask in the order requested by the designer. At this time additional jumper placement and routing occurs, for example the interconnection to the input and output pins, as well as the interconnection of the sections and the digital circuits. The layout designer can also manually enter special options using a light pen. The layout computer based design rule checking program then checks whether the design is compatible with the VLSI-process specifications. After the final layout check, the metal mask is manufactured. The prefabricated wafer is then customized by the metal mask.

Examples of Modem Filter Design

To illustrate one major application for the mask programmable SCF and logic array chip, a 1200 baud half duplex forward channel (with optional 150 baud reverse channel) modem filter which meets the Bell 202 and CCITT V.23 standards has been implemented on this device as a test vehicle. The carrier frequencies for the forward and reverse channels are listed below for both standards.

Bell 202	1200 baud	150 baud
MARK	1200 Hz	390 Hz
SPACE	2200 Hz	490 Hz
CCITT V.23	1200 baud	75 baud
MARK	1300 Hz	390 Hz
SPACE	2100 Hz	450 Hz

The forward channel filter is implemented with a ten-pole bandpass filter realized by cascading 5 second order sections. The same filter is used for both 202 and V.23 since they are both centered at 1700 Hz, and the filter is designed such that the passband will cover the 1200 - 2200 Hz range. Filter specifications, which exceed the Bell/CCITT requirements are given below:

3 dB bandwidth:	>1400 Hz
Adjacent channel rejection:	>50 dB
Group delay variation between MARK and SPACE frequencies for either standards:	< 100 us
Passband ripple:	<+/- 1.5 dB

For the reverse channel, the Bell 202 standard is 150 baud while the CCITT V.23 standard is 75 baud. In general, there is little difference in cost and

complexity between modems incorporating the 75 baud and the 150 baud data rates. So, a modem filter designed to operate up to 150 baud was implemented that will meet both standards. This filter was again designed by using a ten-pole bandpass filter realized by cascading 5 second order sections. The group delay response was compensated for worst case line conditions. In general, the group delay requirement for the reverse channel is not very critical. Bell/CCITT filter specifications listed below are exceeded:

3 dB bandwidth:	> 250 Hz
Adjacent channel rejection:	>50 dB
Group delay variation between MARK and SPACE frequencies:	< 200 us
Passband ripple	< +/- 1 dB

Both forward and reverse channel filters operate from a 3.5795 MHz colorburst crystal to meet the Bell 202 and V.23 standards. The frequency response plots for both filters are shown in Figure 6.

Conclusion

A very versatile semi-custom SCF and logic array is now available for system designers to integrate many analog subsystems. The demand for such a device has existed for some time, but it is only now that the technological advancements in analog MOS make this feasible. Novel SCF and capacitor design and layout techniques are used to supply virtually any type of filter with superior electrical characteristics. With the help of advance design automation tools, design accuracy is assured and typical turnaround time of 8 weeks is achieved. The potential applications for this device in signal processing, telecommunications, data communication and medical signal monitoring are huge. The availability of digital circuits provides the ability to further reduce parts count and add another dimension of flexibility at a low real estate cost. Low cost, fast turnaround and proprietary design are the major benefits to users of this semi-custom SCF and logic array.

Acknowledgement

The authors would like to thank Dr. Gene Weckler and Dr. Hsin-Fu Tseng for their encouragement and support, Mr. Michael Gabler for his software assistance, and Ms. Lois Brubaker and Julie Picarello for their mask design effort.

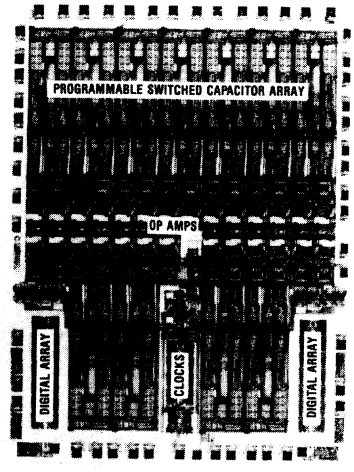


Figure 1:

Layout of Mask Programmable SCF and Logic Array (MPSCF)

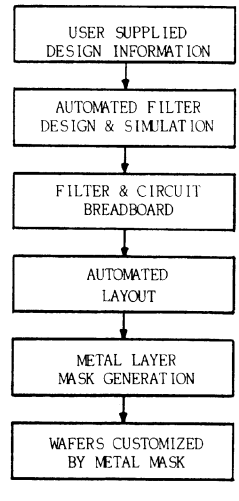


Figure 2:

MPSCF Development Cycle

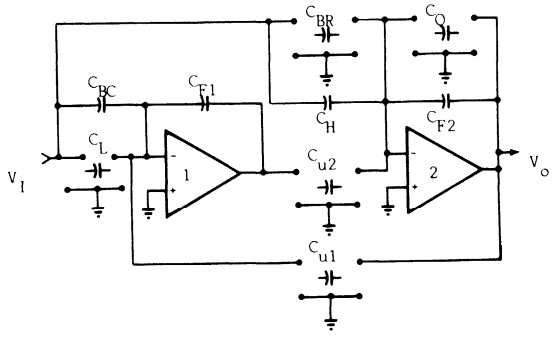
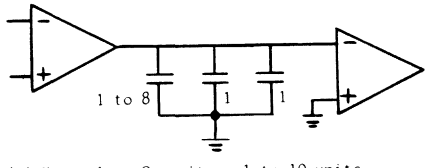
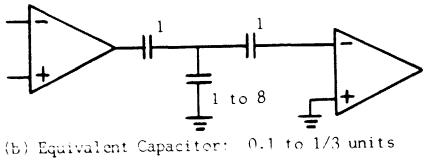


Figure 3: Second Order SCF Building Block



(a) Equivalent Capacitor: 1 to 10 units



(b) Equivalent Capacitor: 0.1 to 1/3 units

Figure 4: Capacitor Scaling Scheme

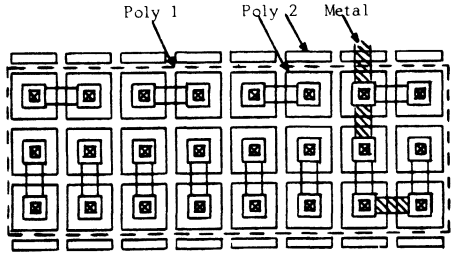
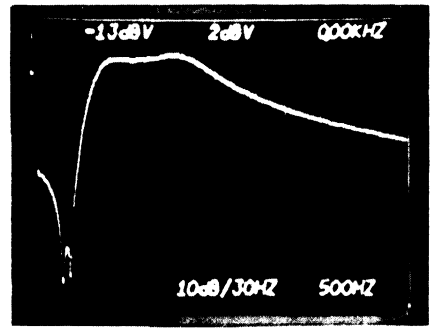
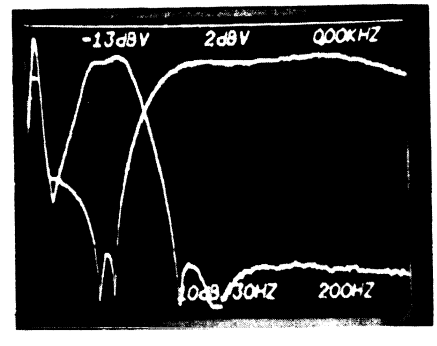


Figure 5: Typical Array of Unit Capacitors



(a) Forward Channel Response



(b) Reverse Channel Response

(plus Forward Channel)

Figure 6: 202/V.23 Modem Filter Response Curves

A Digitally Programmable Switched-Capacitor Universal Active Filter/Oscillator

DOUGLAS B. COX

Abstract—A universal second-order switched-capacitor filter section has been fabricated on an NMOS chip. The device can perform all five basic filter types as well as a sine wave oscillator without external components, while requiring only an external clock. The filter type is determined by selecting one or more of three input pins. The filter response is determined by ten external programming pins which may be either digitally controlled or hard wired.

Introduction

MANY audio frequency filtering requirements are for low volume or specialty filter applications. Since these markets are too small to justify dedicated switched-capacitor standard products or custom designs, they are usually filled by discrete active filters or hybrid universal active filters. These filters require more circuit board area than fully integrated filters and use external components such as resistors and capacitors to determine the frequency response. These filters often require precision components and component trimming. Another disadvantage of discrete filters is that they often require the design engineer to take time out from system development to do filter design.

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A switched-capacitor universal active filter has been developed that can be easily used for low volume and specialty filters. The chip contains a single second-order filter section that can be configured into any of the five basic filter types, low-pass, bandpass, high-pass, notch, and all-pass without requiring any external components, only an external clock. The device has ten TTL compatible programming pins that can be either electrically programmed or hard wired. Filter parameters are selected from a look-up table, eliminating much of the design effort that is required for discrete filters. A block diagram of the switched-capacitor universal active filter chip is shown in Fig. 1.

The filter design, operation, and experimental results are described in this paper.

Filter Design

The universal active filter design is based on the two integrator state variable approach. The many advantages of this configuration have been well reported [1], [2]. The primary advantage is that, except for second-order effects, Q and center frequency (F_0) are independently variable. By modifying the state variable design to have three inputs, one with no integration, one with one integration, and one with two integrations, it is possible to achieve all five of the basic filter types with

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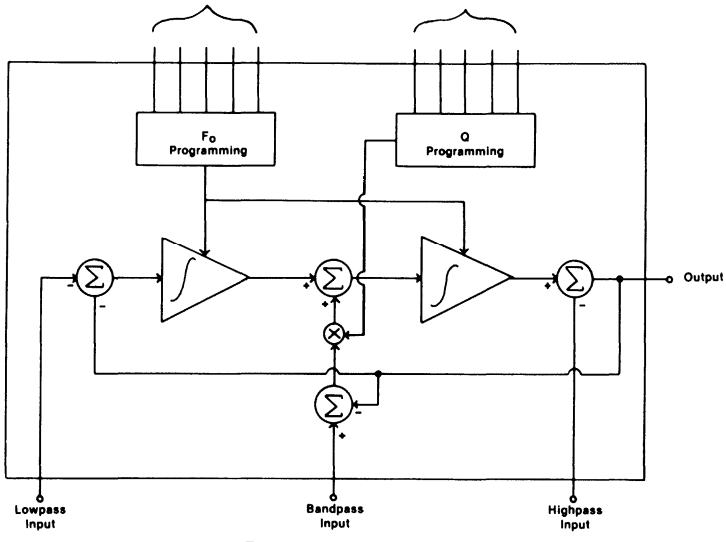

Fig. 1. Functional block diagram.

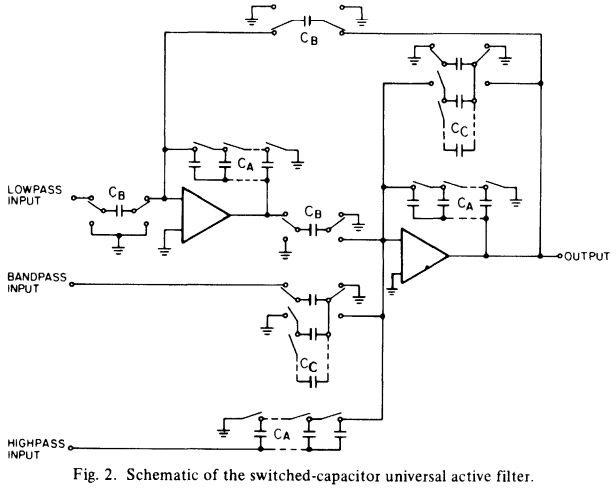

Fig. 2. Schematic of the switched-capacitor universal active filter.

only one circuit. The schematic of that circuit is shown in Fig. 2. The desired filter type may be selected by connecting to the appropriate input. By applying input signal to the low-pass input ($V_{in\,LP}$) only (two integrations), a low-pass filter is selected. By applying the input only to the bandpass input ($V_{in\,BP}$) (one integration), a bandpass filter is selected and if input is only applied to the high-pass input ($V_{in\,HP}$) (no integration), then a high-pass filter is selected. A notch filter is obtained by tying the low-pass and high-pass inputs together, while an all-pass is obtained by tying all three inputs together. The all-pass response is achieved by making the low-pass and high-pass inputs the same polarity (inverting), while the band-pass input is the opposite polarity (noninverting).

The universal filter in Fig. 2 maintains all of the advantages of previously reported programmable filters [1], [2] while eliminating two of the disadvantages. First, by accomplishing the Q termination with a switched-capacitor resistor around op amp 2, it is possible to eliminate the need for a third op amp, and secondly, by eliminating the third op amp, the parasitic pole caused by that op amp is eliminated. This significantly improves the low Q performance.

The operation of the circuit can be most easily explained by

deriving the simplified transfer function from Fig. 2:

$$V_{out}(S) = -\frac{V_{inHP}S^2 - V_{inBP}\dfrac{F_C C_C}{C_A}S + V_{inLP}\left(\dfrac{F_C C_B}{C_A}\right)^2}{S^2 + \dfrac{F_C C_C}{C_A}S + \left(\dfrac{F_C C_B}{C_A}\right)^2} \quad (1)$$

where V_{inHP}, V_{inBP}, and V_{inLP} are the high-pass, bandpass, and low-pass inputs, respectively. By comparing this transfer function to the general-purpose second-order transfer function [3],

$$V_{out}(s) = \frac{V_{inHP}S^2 + V_{inBP}\dfrac{\omega_0}{Q}S + V_{inLP}\omega_0^2}{S^2 + \dfrac{\omega_0}{Q}S + \omega_0^2}, \quad (2)$$

it is possible to solve for the approximate values of Q and ω_0:

$$Q = \frac{C_B}{C_C} \quad (3)$$

$$\frac{F_C}{\omega_0} = \frac{C_A}{C_B} \quad (4)$$

Thus, to the first-order, Q can be controlled by adjusting C_C and F_0 can be controlled by adjusting C_A. As can be seen from Fig. 2, both C_A and C_C are determined by switching capacitors in and out from a parallel capacitor array. In the C_A case, the unused capacitors are grounded to minimize glitches on the output when F_0 is changed. Glitches are not a problem when changing Q because the Q determining capacitor C_C is discharged every sample. In order to improve Q accuracy, C_B is made up of 20 units of capacitance, approximately 0.2 pF each. Thus, it is possible to do Q's up to 20 with good accuracy. For Q's above 20, the Q capacitor C_C must be smaller than 0.2 pF. This results in a reduced accuracy for higher Q's of approximately ±10 percent.

Since (1) and (2) do not take into consideration the sampled data effects on the filter, it is necessary to take them into account to determine the exact capacitor values. Due to the sample rate to center frequency ratio being at least 25:1 or greater, these effects are small but still significant. The correct transfer function for the circuit of Fig. 2 is

$$V_{out}(z) = -\frac{V_{inHP}[z^2 - 2z + 1] - V_{inBP}\dfrac{C_C}{C_A}[z - 1] + V_{inLP}\left(\dfrac{C_B}{C_A}\right)^2 Z}{Z^2\left[1 + \dfrac{C_C}{C_A}\right] + Z\left[\left(\dfrac{C_B}{C_A}\right)^2 - \dfrac{C_C}{C_A} - 2\right] + 1} \quad (5)$$

As can be seen from (5), there is a second-order effect of C_C/C_A that effects both Q and F_0. Though it is possible to compensate for this effect by adjusting C_A and C_C for a specific value of Q and F_0, they cannot be matched for all values of Q and F_0. Thus Q and F_0 programming cannot be totally independent. Since the term C_C/C_A decreases as the sample rate to center frequency ratio and Q increase, these effects are significant only on the lower Q and lower sample rate to center frequency ratio values. Measurements of these errors are shown in the test results section.

TABLE I
INPUT PIN CONNECTION LIST FOR THE VARIOUS FILTER TYPES

Filter Type	Connections VinLP	VinHP	VinBP
Lowpass	Vin	GND	GND
Highpass	GND	Vin	GND
Bandpass	GND	GND	Vin
Notch	Vin	Vin	GND
Allpass	Vin	Vin	Vin
Oscillator	GND	GND	OUTPUT

DEVICE OPERATION

In order to use the digitally programmable universal active filter, three operating parameters must be selected: filter type, Q, and sample frequency to center frequency ratio. The filter type is selected by wiring the three input lines that are shown in Fig. 2. As described in the previous section, all five basic filter types may be selected by connecting one or more of the three input lines to the input signals. An input connection list is shown in Table I. It is necessary to tie all unused inputs to ground to reduce crosstalk. These inputs are all referenced to virtual ground nodes internal to the chip, thus making any deterioration in filter response due to grounding the unused pins insignificant. Besides producing the five basic filter types, the chip can also be configured to provide a sine wave oscillator. The nominal gain for the bandpass mode is 0 dB; however, one Q, the Q of 40 (code 11101) has a gain of 0.5 dB. By connecting the output to the bandpass input using this Q, the filter will oscillate at the center frequency of the bandpass filter.

With the addition of two external resistors, it is also possible to generate elliptic low-pass and high-pass filters. The connections for an elliptic low-pass is shown in Fig. 3. An elliptic high-pass may be constructed by swapping the low-pass and high-pass connections to the resistor divider. The notch frequency for the low-pass case is

$$F_z = \sqrt{\frac{R1 + R2}{R2}} \times F_0 \quad (8)$$

and for the high-pass case

$$F_z = \sqrt{\frac{R2}{R1 + R2}} \times F_0. \quad (9)$$

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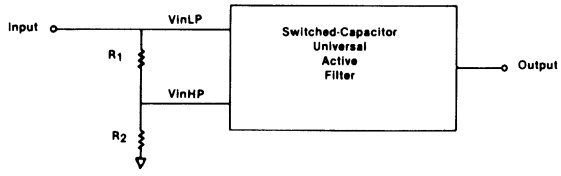

Fig. 3. Connections for an elliptic low-pass configuration.

TABLE II
Q, F_0 Programming Table

Q	CODE $Q4 \ldots Q0$	F_S/F_0	CODE $F_04 \ldots F_00$
.57	00000	100.0	00000
.65	00001	95.6	00001
.71	00010	91.4	00010
.79	00011	87.4	00011
.87	00100	83.6	00100
.95	00101	79.9	00101
1.05	00110	76.4	00110
1.2	00111	73.1	00111
1.35	01000	69.9	01000
1.65	01001	66.8	01001
1.95	01010	63.9	01010
2.2	01011	61.1	01011
2.5	01100	58.4	01100
3.0	01101	55.9	01101
3.5	01110	53.4	01110
4.25	01111	51.1	01111
5.0	10000	48.9	10000
5.8	10001	46.7	10001
7.2	10010	44.7	10010
8.7	10011	42.7	10011
10.0	10100	40.9	10100
11.5	10101	39.1	10101
13.0	10110	37.4	10110
15.0	10111	35.7	10111
17.5	11000	34.2	11000
19.0	11001	32.7	11001
23.0	11010	31.2	11010
28.0	11011	29.9	11011
35.0	11100	28.6	11100
40.0	11101	27.4	11101
80.0	11110	26.2	11110
150.0	11111	25.0	11111

The Q and center frequency selection is controlled by ten TTL and CMOS compatible digital inputs, five for the Q and five for the center frequency. The Q and center frequency may be either digitally controlled or the pins may be hard wired for a fixed response. The programming time is less than 1 μs, though consideration must be given to the impact of stored energy in the filter when programming occurs as well as the delay time of the new filter after programming. These parameters will both affect the amount of time the new filter will require to give a valid output.

The five Q control lines can be used to select 32 different Q's from 0.57 to 150. The five center frequency control lines are used to select from 32 logarithmically spaced clock to center frequency ratios covering two octaves. Table II lists the available Q and center frequency values for the various digital inputs.

By balancing the bandpass input switched-capacitor resistor with the Q controlling switched-capacitor resistor, the bandpass gains (except for $Q = 40$) have all been set to 0 dB. The low-pass and high-pass filters are set for unity gain in the flat-band portion of their responses, so there will be peaking near the corner frequency on higher Q filters. By setting the gains in this fashion, notch and all-pass filters can be obtained by simply applying input signals to more than one input.

Test Results

A die photomicrograph of the digitally programmable universal active filter is shown in Fig. 4. The device was fabricated in a double-poly NMOS process and has a die size of 100 X 116 mils.

Demonstration of the eight possible operating modes is shown in Fig. 5. All five of the basic filter types are included as well as low-pass and high-pass elliptic filters and the sine wave oscillator output. The oscillator output is shown with ± 10 V supplies. The stair step response characteristic of switched-capacitor filters is visible. Sine wave distortion is down 38 dB. The all-pass filter photograph displays the slight amplitude distortion caused by sampled data effects. This distortion varies from 0.2 dB for the lowest Q's to over 1 dB for Q's greater than 20.

Examples of the Q and center frequency programming of the device are shown in Fig. 6. Fig. 6(a) shows all 32 of the possible center frequency values that are available for a given clock rate. The values are logarithmically spaced over two octaves. Fig. 6(b) shows the spread available on the Q values. Q's of 0.57, 5, and 40 are shown. Both of these photos demonstrate the bandpass mode of operation.

A summary of the typical operating parameters is shown in Table III. The dynamic range is improved over previous designs

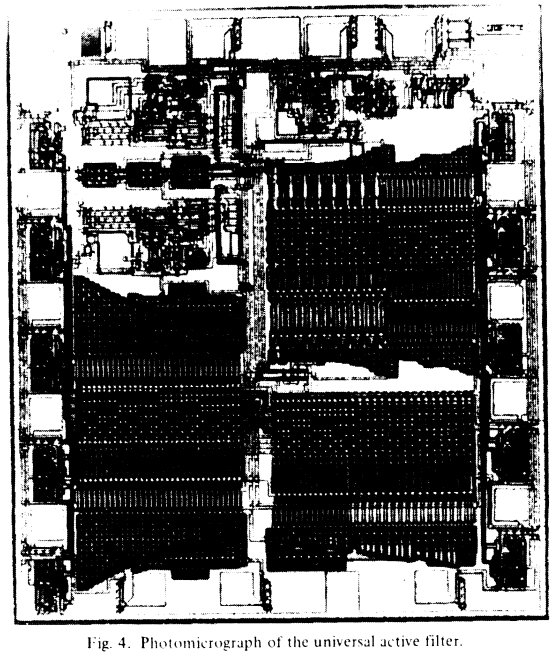

Fig. 4. Photomicrograph of the universal active filter.

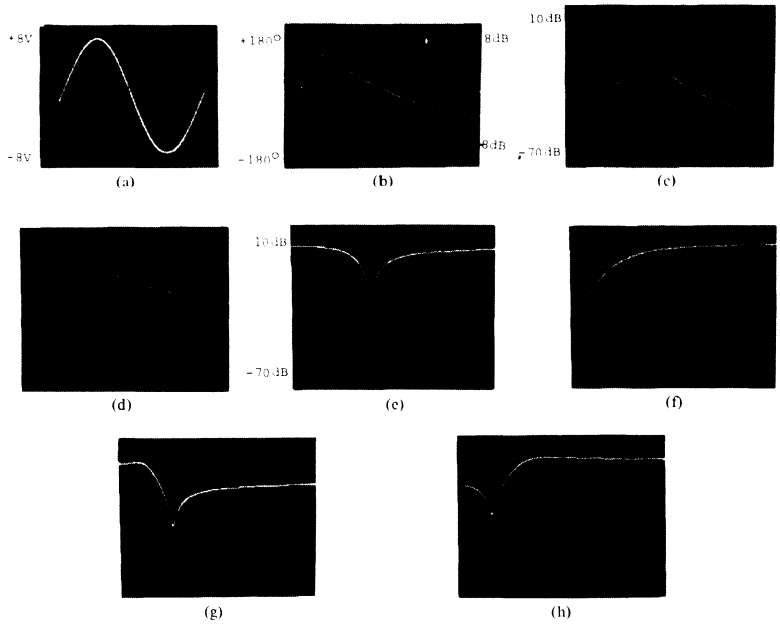

Fig. 5. Operating modes of the switched-capacitor filter/oscillator. (a) Programmable oscillator output. (b) All-pass filter. (c) Bandpass filter. (d) Low-pass filter. (e) Notch filter. (f) High-pass filter. (g) Low-pass elliptic filter. (h) High-pass elliptic filter.

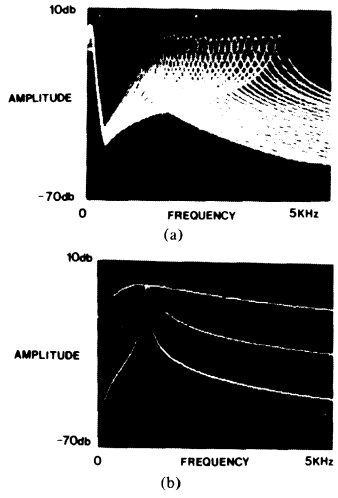

Fig. 6. Q and F_0 programming. (a) 32 center frequencies over two octaves with one input clock. (b) Q's of 0.57, 5, and 40.

TABLE III

Power Supplies	±4 to ±10V
Operating Current	3.5 ma
Dynamic Range (Q = 1)	85 dB
Dynamic Range (Q = 40)	75 dB
Sample Rate Range	10 Hz to 500 KHz
Maximum Voltage Swing	14V p-p
Distortion	0.2%
PSRR (Q=1)	10 dB
Sample Rate Feedthrough	30 mV
Offset Voltage	100 mV

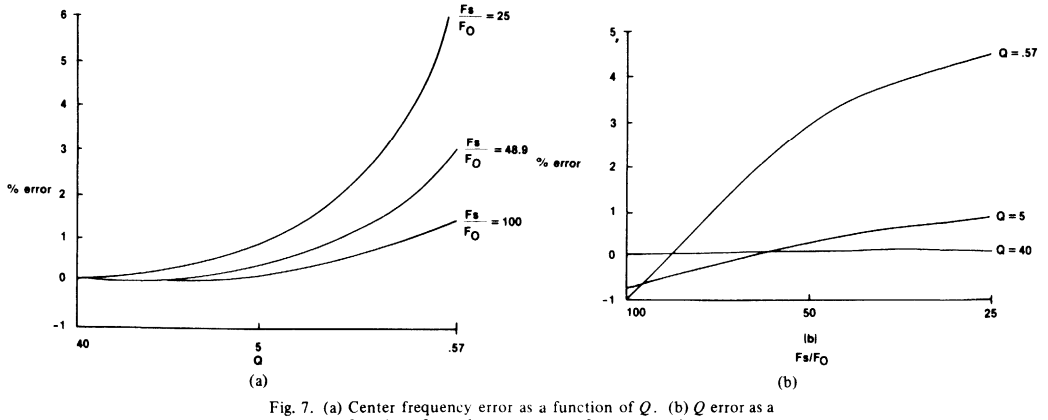

Fig. 7. (a) Center frequency error as a function of Q. (b) Q error as a function of sample rate to center frequency ratio.

through both op amp design improvements and the elimination of a third op amp. Low frequency operation is also greatly improved through the elimination of the parasitic pole needed for biasing the third op amp. The dynamic range listed is for F_0 = 1 kHz, F_s = 100 kHz and rms signal to rms noise up to one half the sample rate. The Q and clock to corner frequency ratio values listed in Table II are the nominal values. Since the second-order effects caused by sampling increase as the Q decreases, it is impossible to have both Q and center frequency programming totally independent. The sample rate to center frequency ratio values are designed to be within a 1 percent tolerance for all values of Q greater than five and the Q values are designed to be within a 1 percent tolerance for a clock to corner ratio of 100. Graphs describing this second-order effect are shown in Fig. 7. Fig. 7(a) shows the error in center frequency as a function of Q for a sample rate to center frequency

ratio of 25, 48.9, and 100. Fig. 7(b) shows the Q error as a function of sample rate to center frequency ratio for Q's, of 0.57, 5, and 40. These measured values are all within 20 percent of the theoretical error.

Summary

A digitally programmable second-order switched-capacitor universal active filter/oscillator has been fabricated on a single NMOS chip. All five basic filter types as well as a sine wave oscillator are available without external components. The device can be used for audio frequency filtering applications that require either a digitally programmable response or a hard wired fixed response.

References

[1] D. B. Cox, L. T. Lin, R. S. Florek, and H. F. Tseng, "A real-time programmable switched-capacitor filter," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 972-977, Dec. 1980.

[2] D. J. Allstot, R. W. Brodersen, and P. R. Gray, "An electrically programmable switched-capacitor filter," *IEEE J. Solid-State Circuits*, vol. SC-14, pp. 1034-1041, Dec. 1979.

[3] G. E. Tobey, G. G. Graeme, and L. P. Huelsman, *Operational Amplifiers, Design, and Applications.* New York: McGraw-Hill, 1971, pp. 285-286.

Douglas B. Cox received the B.S.E.E. degree from the University of Utah, Salt Lake City, and the M.S.E.E. degree from the University of Southern California, Los Angeles.

He was a member of the Technical Staff at Hughes Aircraft Corporation, where he designed and characterized charge-coupled devices for use in infrared systems. Since joining EG&G Reticon, Sunnyvale, CA, in 1977 he has been involved with the design of analog signal processing integrated circuits using switched-capacitor filters. He is currently the Design Section Head for switched-capacitor filter products.

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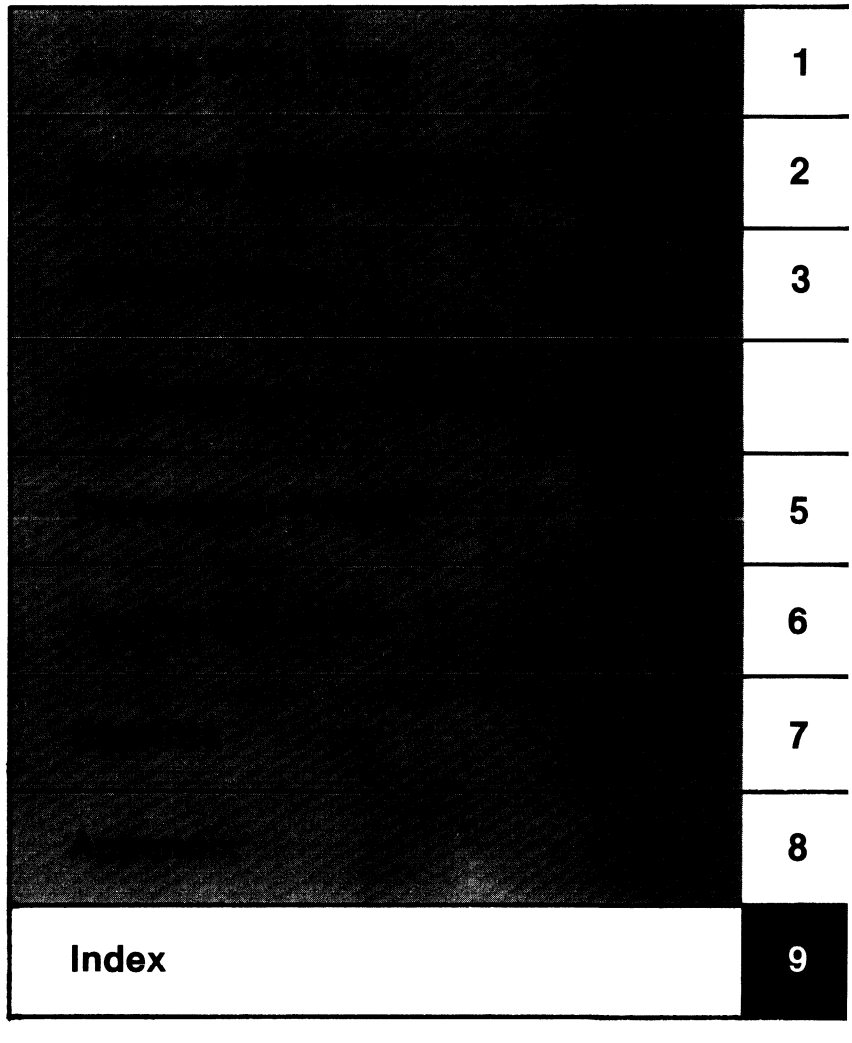

PRODUCT CROSS REFERENCE

PRODUCT NAME	SECTION
R5106	Delay Lines
R5107/8	Delay Lines
R5601A	Transversal Filters
R5602A	Transversal Filters
R5604/5/6	Switched Capacitor Filters
R5609/13	Switched Capacitor Filters
R5611/12	Switched Capacitor Filters
R5614/15/16	Switched Capacitor Filters
R5620	Universal Active Filters
R5621/22	Universal Active Filters
R5626	Universal Active Filters
R5630/31	Modem Filters
R5632	Modem Filters
R5633	Modem Filters
TAD32	Transversal Filters

Notes

Notes

Notes

TABLE I: ABSOLUTE MAXIMUM/MINIMUM RATINGS

	Min	Max	Units
Input Voltage—any terminal with respect to substrate(1)	-.4	21	V
Input/Output current—any terminal (externally forced)(2)		10	mA
Power Dissipation(3)	500		mW
Storage Temperature	-55	125	°C
Temperature under maximum bias	0	70	
Temperature under ½ maximum bias	0	125	

CAUTION: Observe MOS Handling & Operating Procedures

(1) Although devices are internally gate protected to minimize the possibility of static damage, MOS handling precautions should be observed. Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

(2) It is possible to exceed the maximum voltage limit when forcing current, especially on the inputs.

(3) Under worse case loads and temperature, the package limitations prevail. In normal modes of operation, total power dissipated is a combination of Quiescent Power (e.g., $I_{QSS} V_{SS} + I_{ODD} V_{DD}$) plus a percentage of output load power which reflects the efficiency of the output driver. The power dissipation of the substrate will exceed this plastic package limit.

NOTE: The temperature under bias rating applies to all Reticon analog products, including delay lines, switched capacitor filters, transversal filters, etc. If different ratings are required, please consult the factory.